ultrasponder

SEVENTH FRAMEWORK PROGRAMME

Workshop ESSCIRC

Low-Power Data Acquisition System For Very Small Signals At Low Frequencies With12-Bit-SAR-ADC

17. September 2010

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IMST

Outline

→ System Overview

→ Analog-Front-End

- Chopper-Amplifier
- Anti-Aliasing-Filter
- Measurement Results

→ Charge Scaling SAR-ADC

- ADC-Concept
- Measurement Results

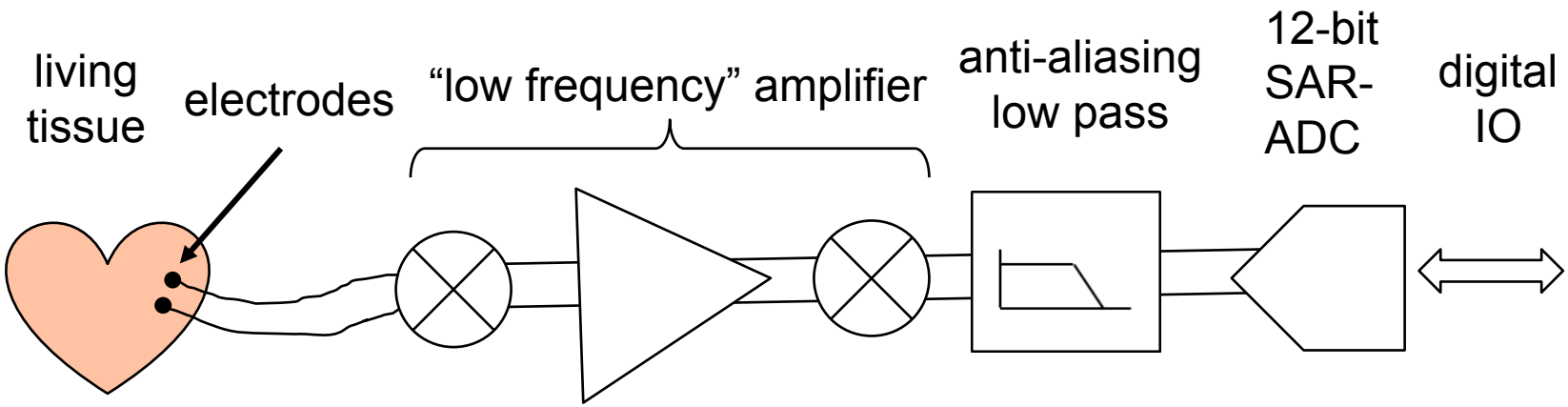
→ System Summary

Data Acquisition System Overview

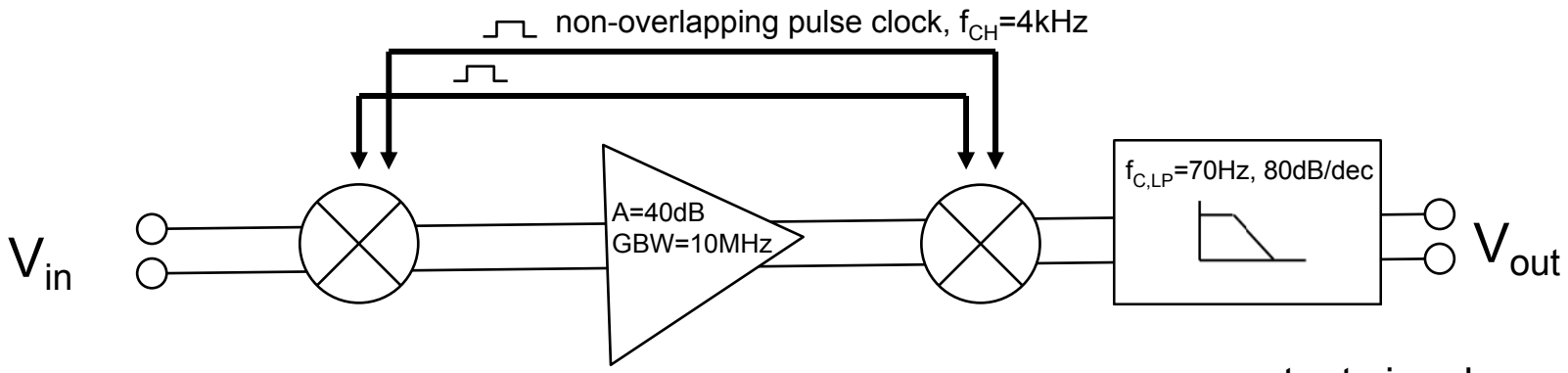
Purpose: sensor frontend of the Ultrasponder-implant

Problems with biomedical signals:

- at very low frequencies 1/f noise dominates in amplifiers and overlays very small signals
- dc-offsets in amplifiers at very high gain distort or even destroy these signals



Solution: use a chopping amplifier



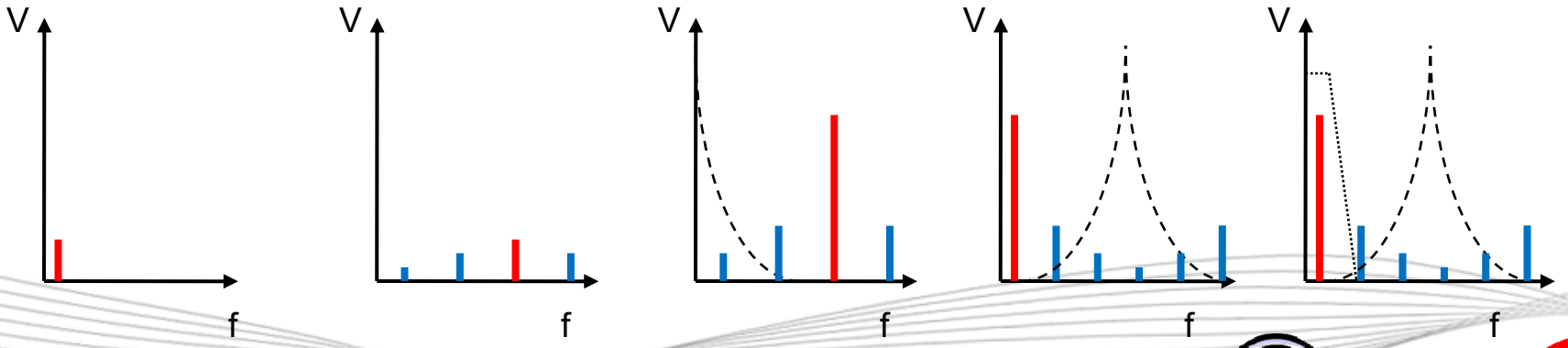
Input Signal below expected 1/f-noise floor

modulation of input signal up to higher frequency by a square-wave → “chopping”

amplification => high band-width required due to square-wave spectrum

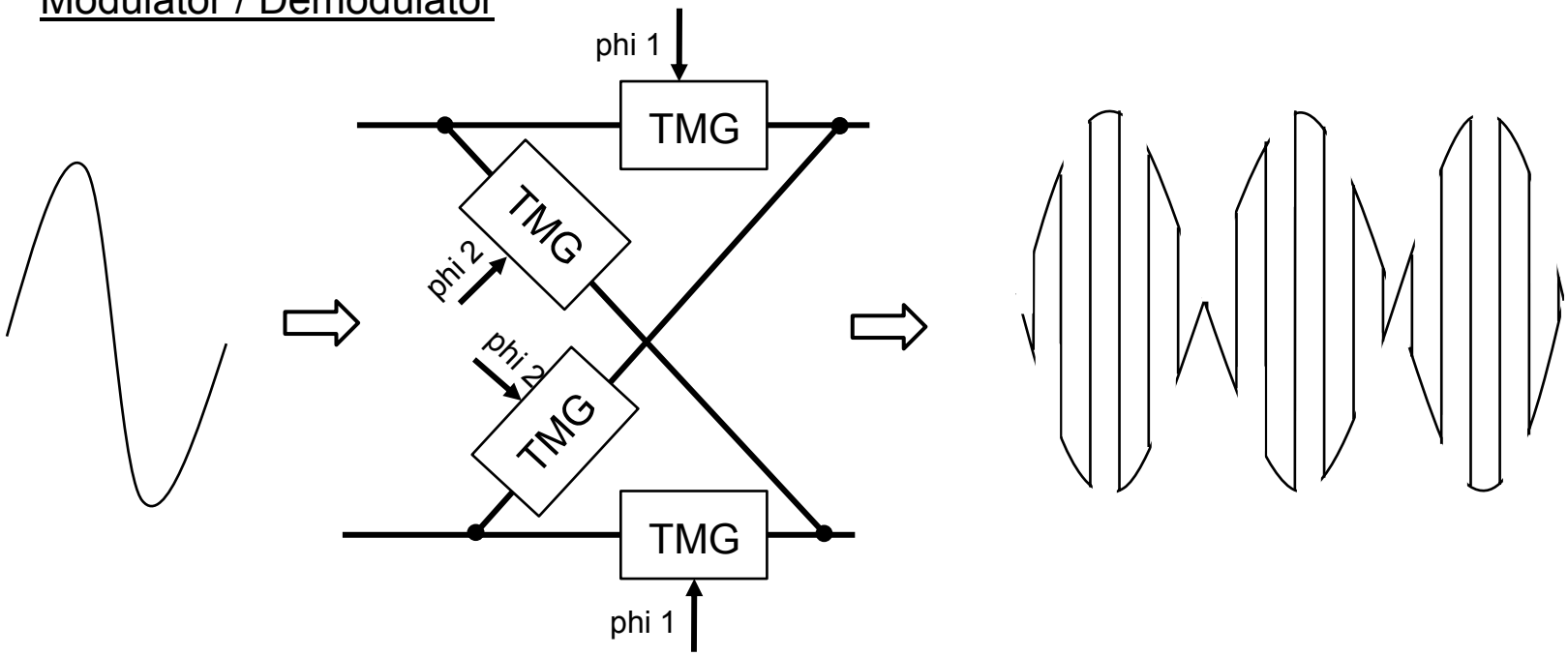
demodulation by the same square-wave

output signal contains the amplified input and undesired signals at high frequencies => low-pass filtering required!

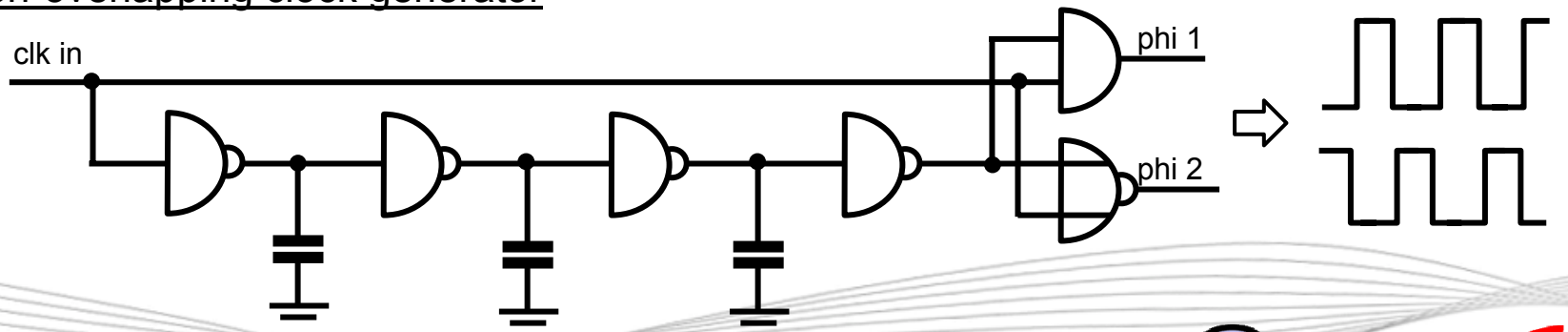


Realization of Chopper-Elements

Modulator / Demodulator



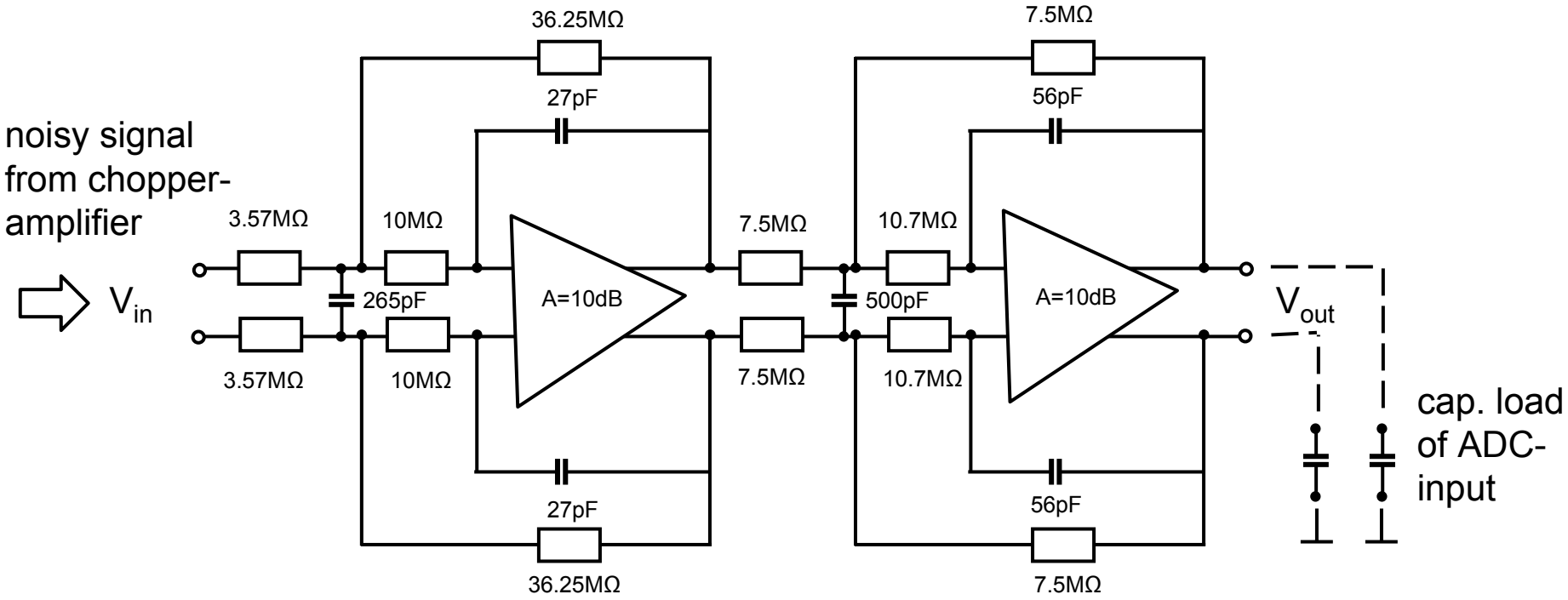
Non-overlapping clock generator



Active LP- Filter – Fully Differential Multiple Feedback

Anti-Aliasing-Low-Pass-Filter Requirements

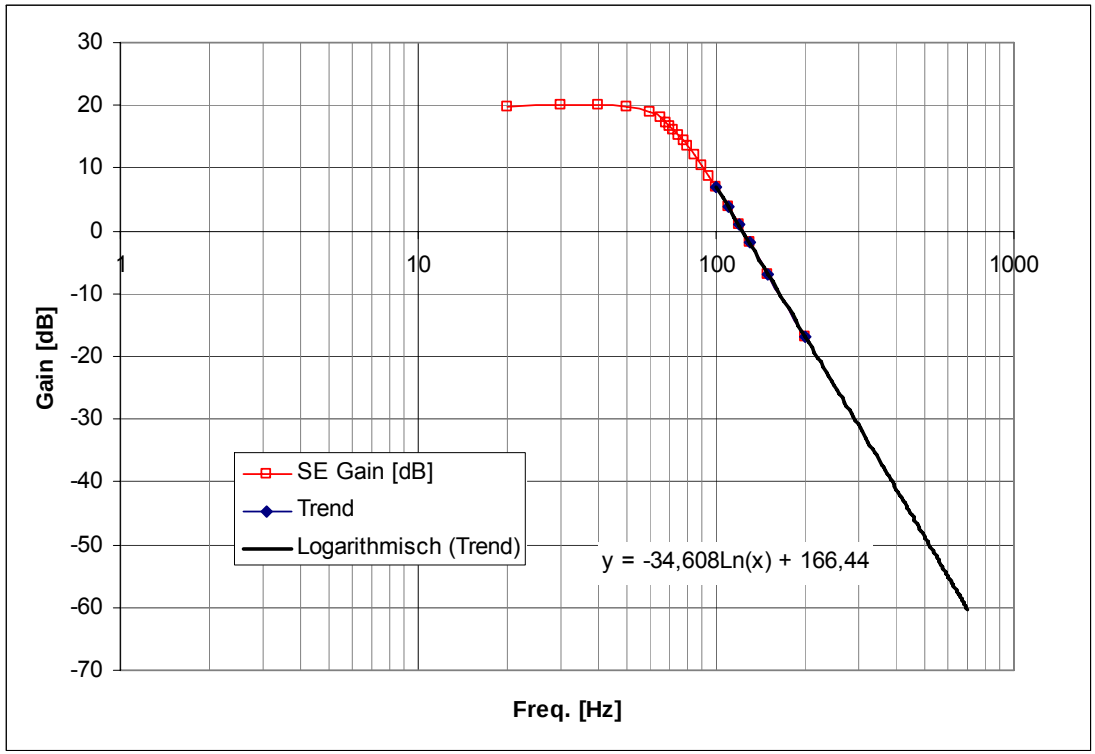
- 20dB gain in pass-region
- cut-off-frequency $f_{C,3dB}$=70Hz => large external passive elements required
- filter suppression of 72.24dB at least required for 12 bit resolution in ADC

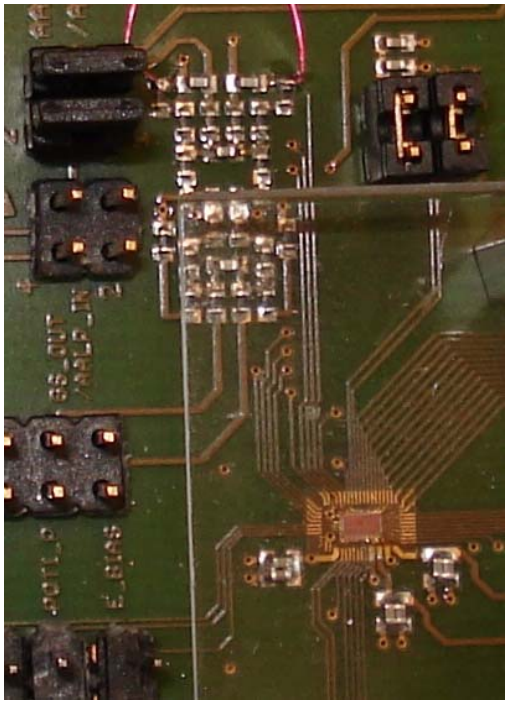


Anti-Aliasing-Filter: frequency plot from lab-results

Verification of parameters by measurement

- 20dB Gain in pass-region
- cut-off-frequency $f_{C,3dB}$=70Hz
- cut-off-steepness 80dB/decade due to 4th filter order

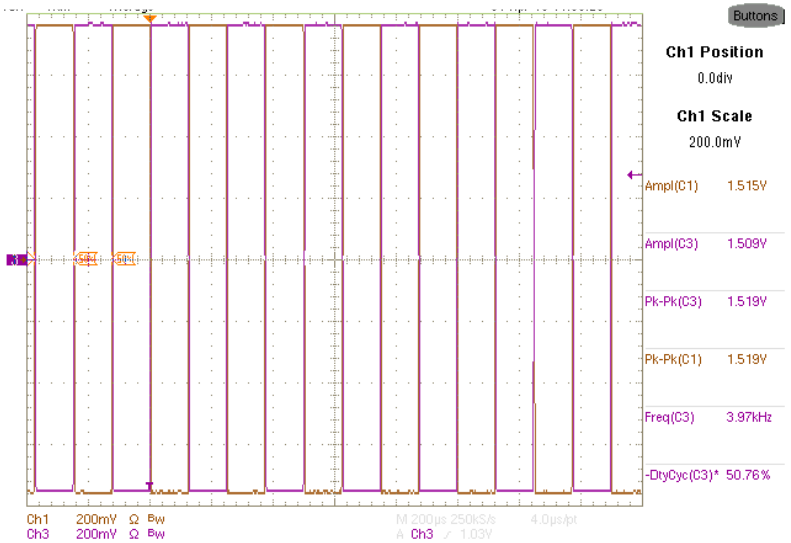




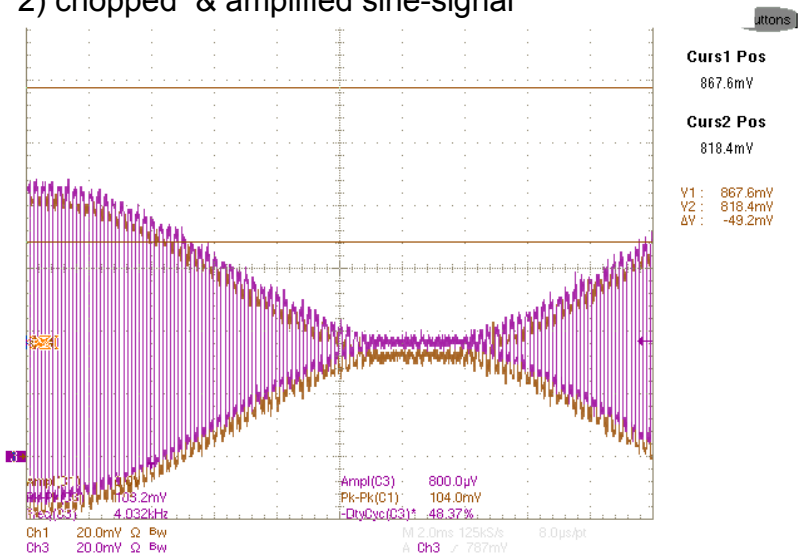
ext. filter-elements on testboard

Chopping in time domain: lab results

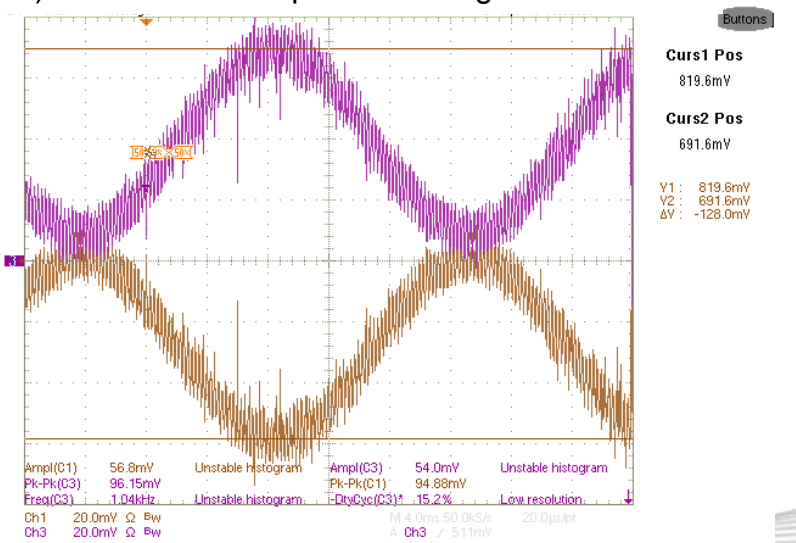
1) pulse-clock source



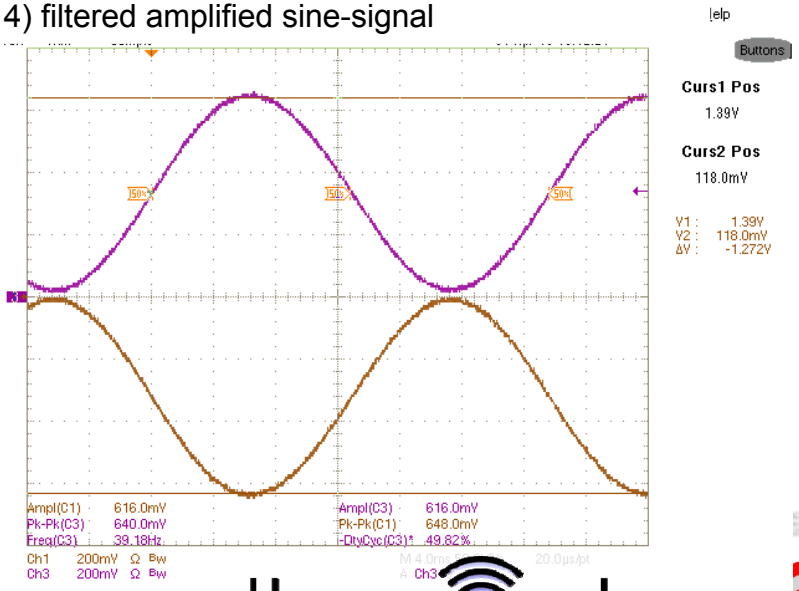
2) chopped & amplified sine-signal



3) demodulated amplified sine-signal



4) filtered amplified sine-signal



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→ System Overview

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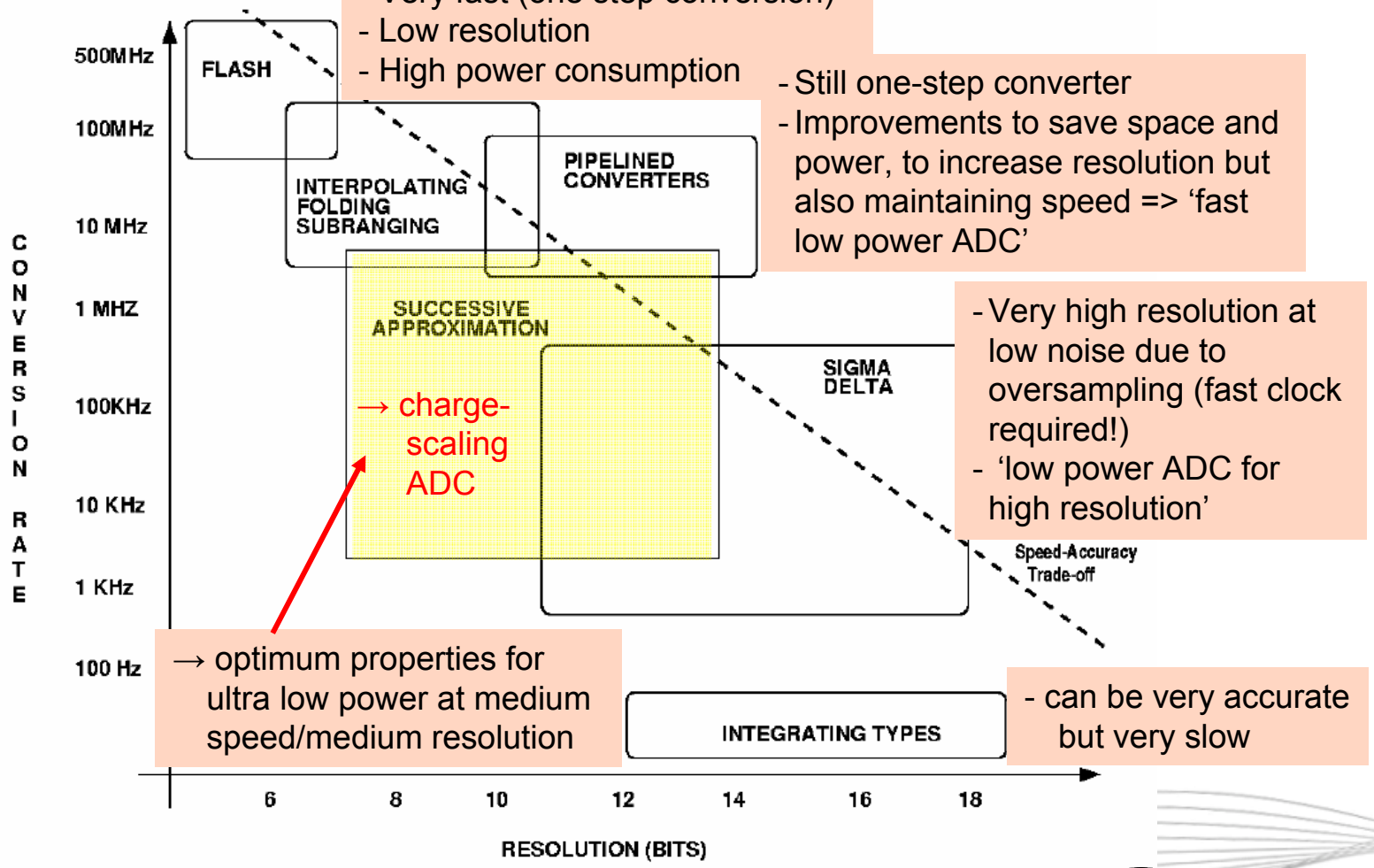
→ **Charge Scaling SAR-ADC**

- **ADC-Concept**
- **Measurement Results**

→ System Summary

Overview of ADC-Concepts: Speed vs Resolution

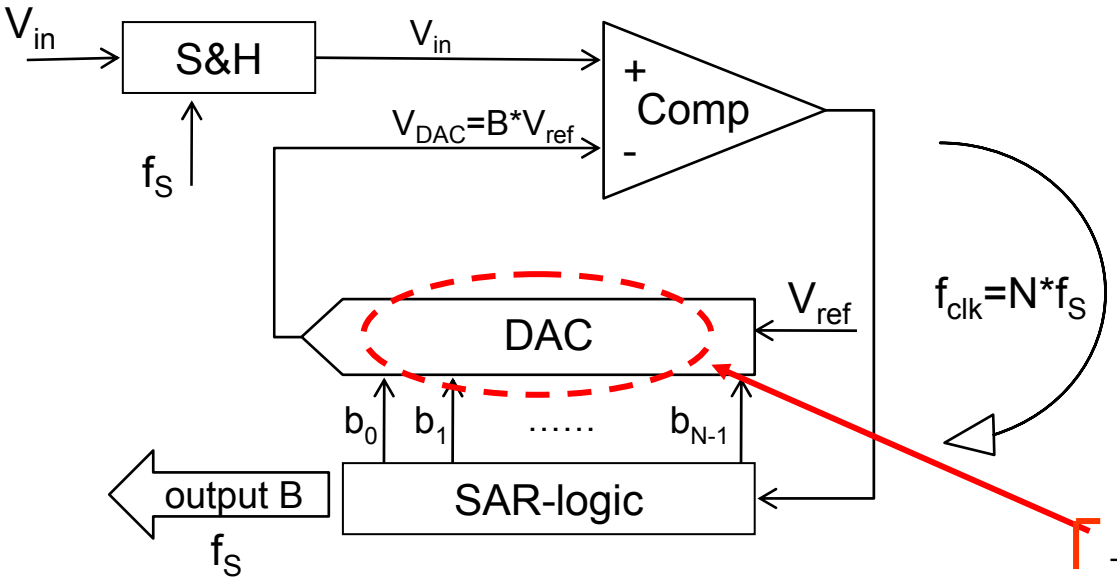
Targeted: 12bit, f_S<50kS/s, V_{ref}=1.5V, f_{clk}=1MHz



Source: Sansen, Analog Design Essentials, p. 209

Successive-Approximation-Register-ADC (SAR)

General SAR-structure

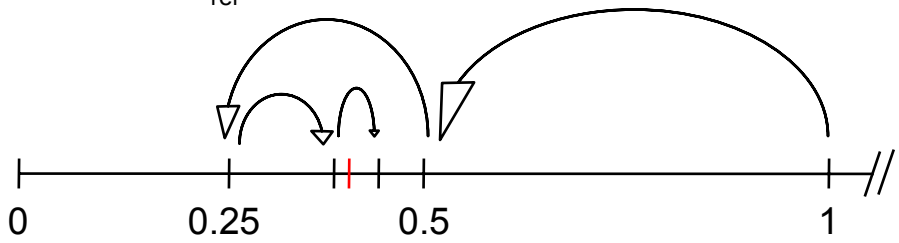


Source: Johns/Martin, Analog Integrated Circuit Design

→ here the DAC is realized as a charge-scaling capacitor-array
→ advantage: DAC also acts as S&H, very low power

General SAR-algorithm

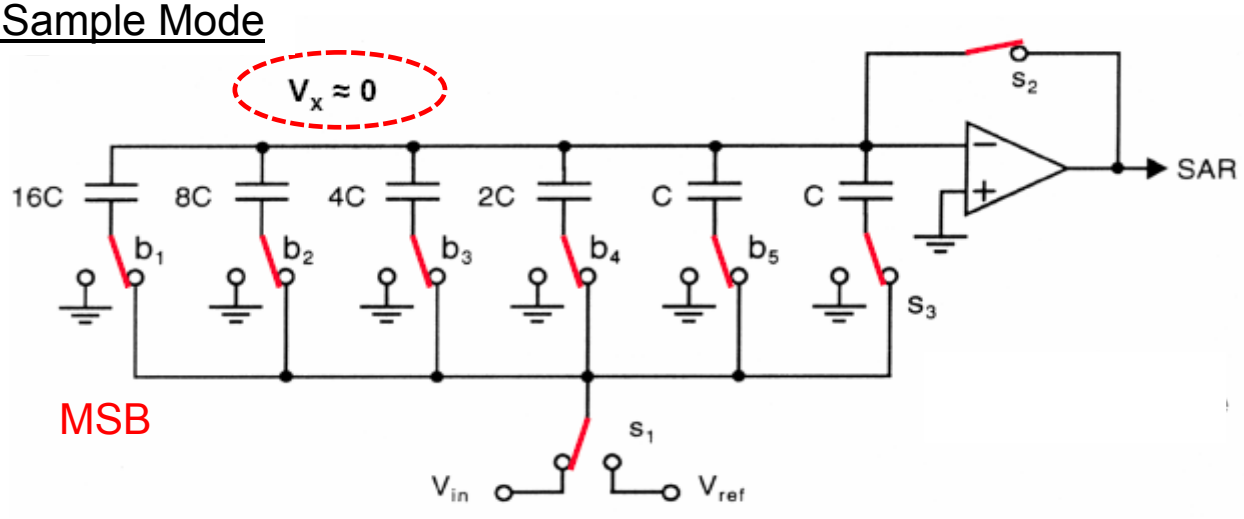
Example: find 0.4 V_{ref}



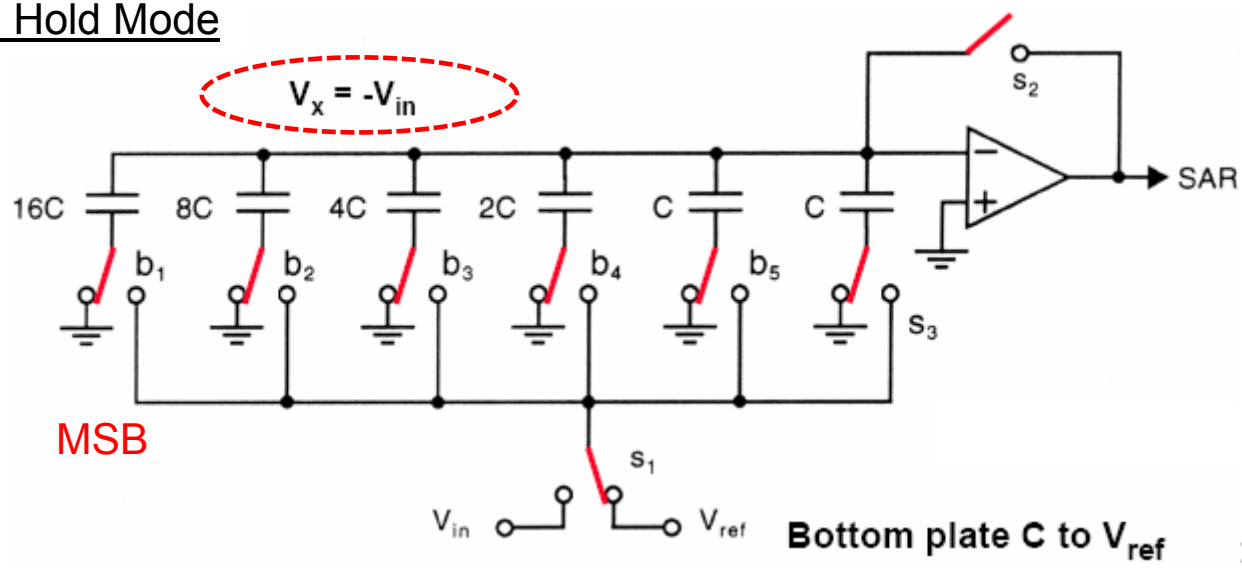
axis normalized to $V_{ref}/2$

SAR-ADC with Charge Scaling DAC (1)

1. Sample Mode



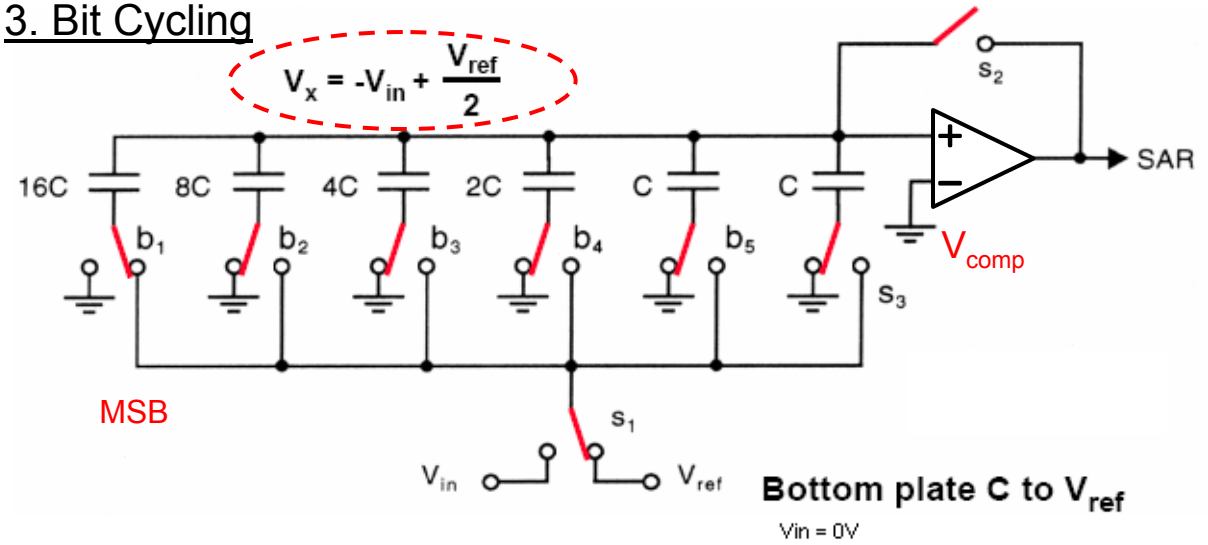
2. Hold Mode



Source: Sansen, Analog Design Essentials

SAR-ADC with Charge Scaling DAC (2)

3. Bit Cycling



Cycling principle:

If $V_x > V_{ref}/2^i$: $b_i = 1$

$\Rightarrow$ leave C_{bi} to V_{ref}

if $V_x < V_{ref}/2^i$: $b_i = 0$

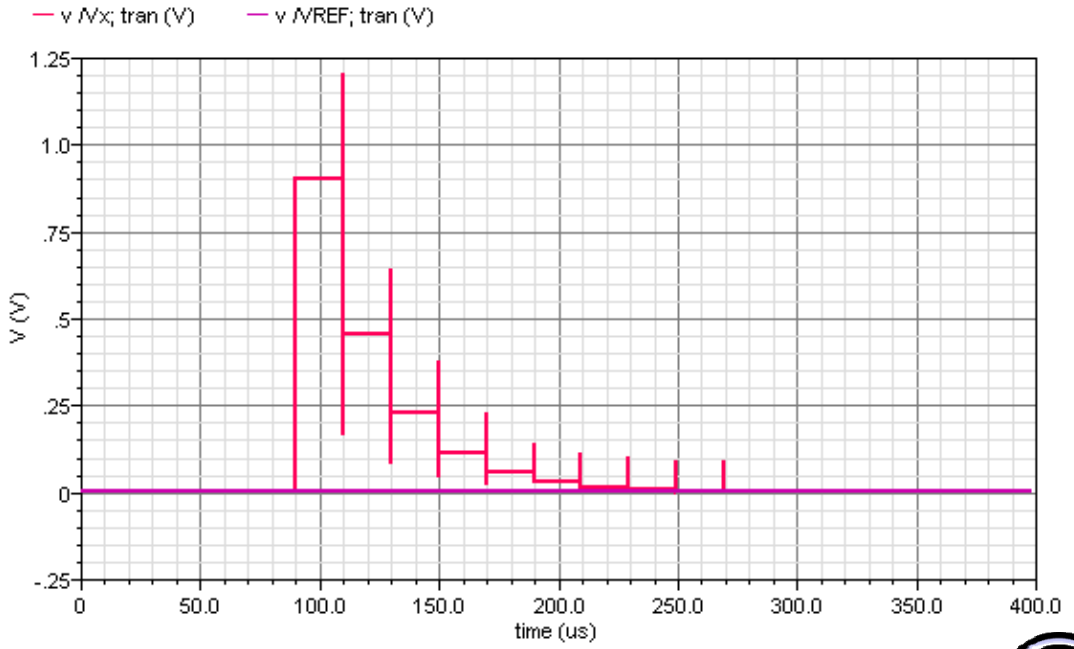
$\Rightarrow$ leave C_{bi} to GND

Source: Sansen, Analog Design Essentials

V_{in}=0V

results in

B='0000000000'

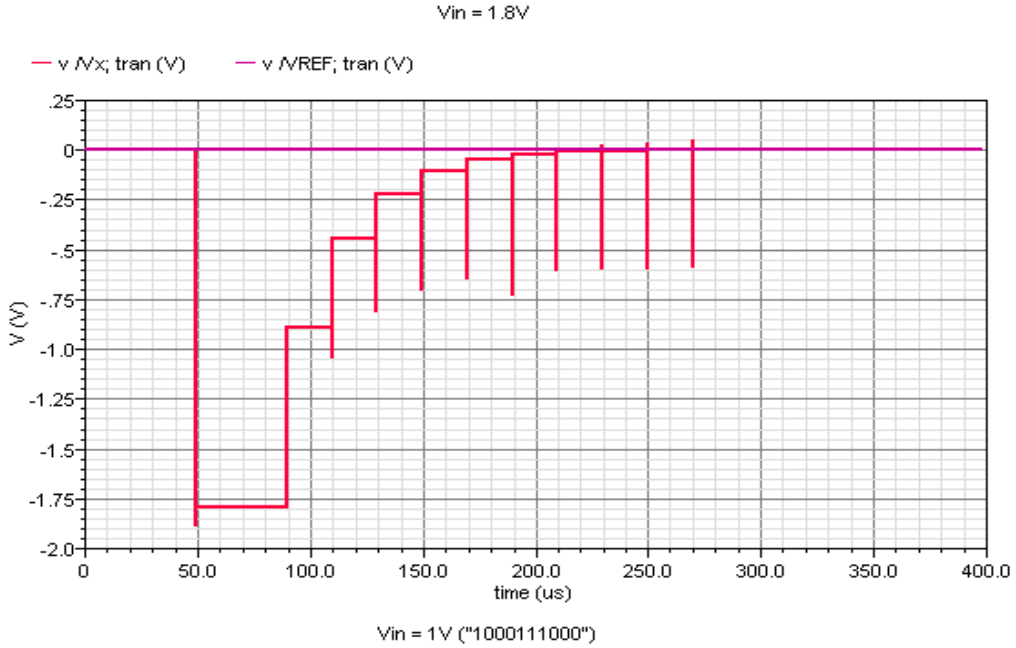


SAR-ADC with Charge Scaling DAC (3)

V_{in}=1.8V

results in

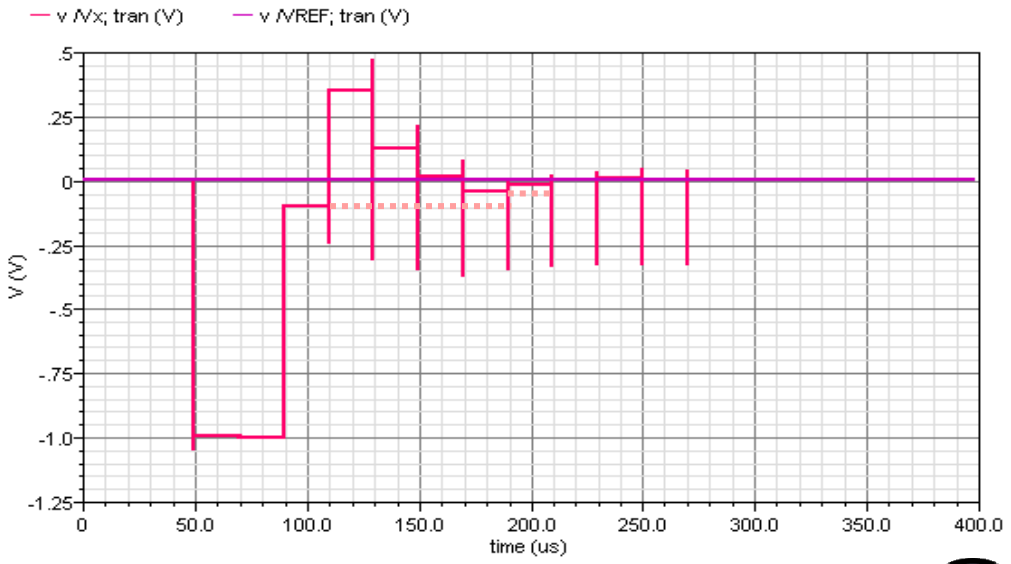
B='1111111111'



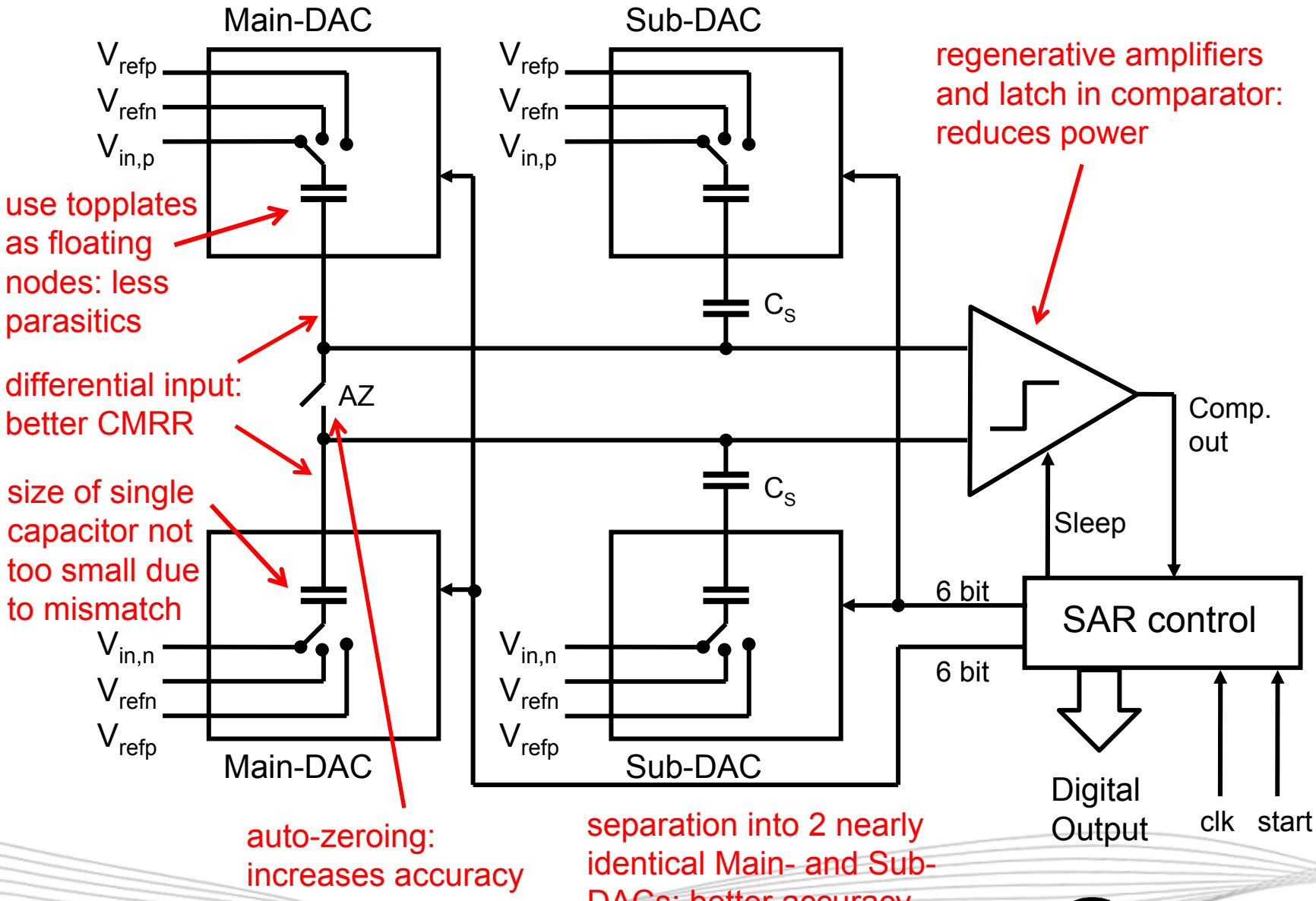
V_{in}=1.0V

results in

B='1000111000'

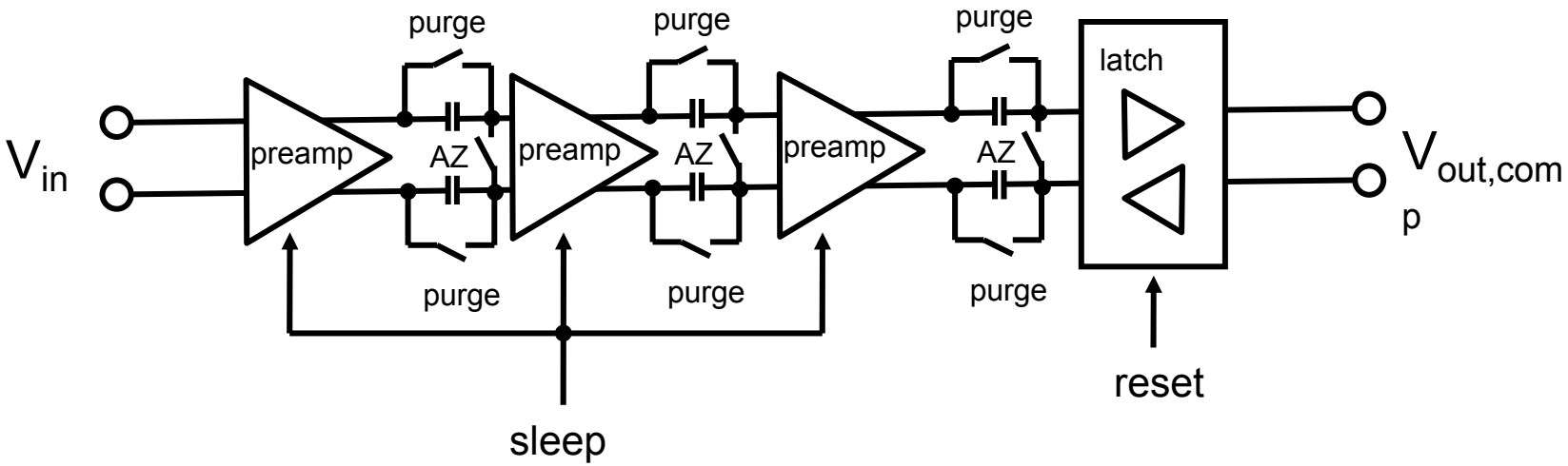


Design Improvements of the ADC for Ultrasponder



Design of the Comparator with Autozero

- single-stage preamplifiers increase V_{in}-sensitivity to 180uV (= V_{LSB}/2) @ settling-time t_{settle}< 500ns (maximum system-clock f_{clk}=1MHz)



A 4-step autozero-cycle is preceding every conversion:

1. Each preamp is shorted at its input. A short closing of the purge-switches discharges the autozero-capacitors

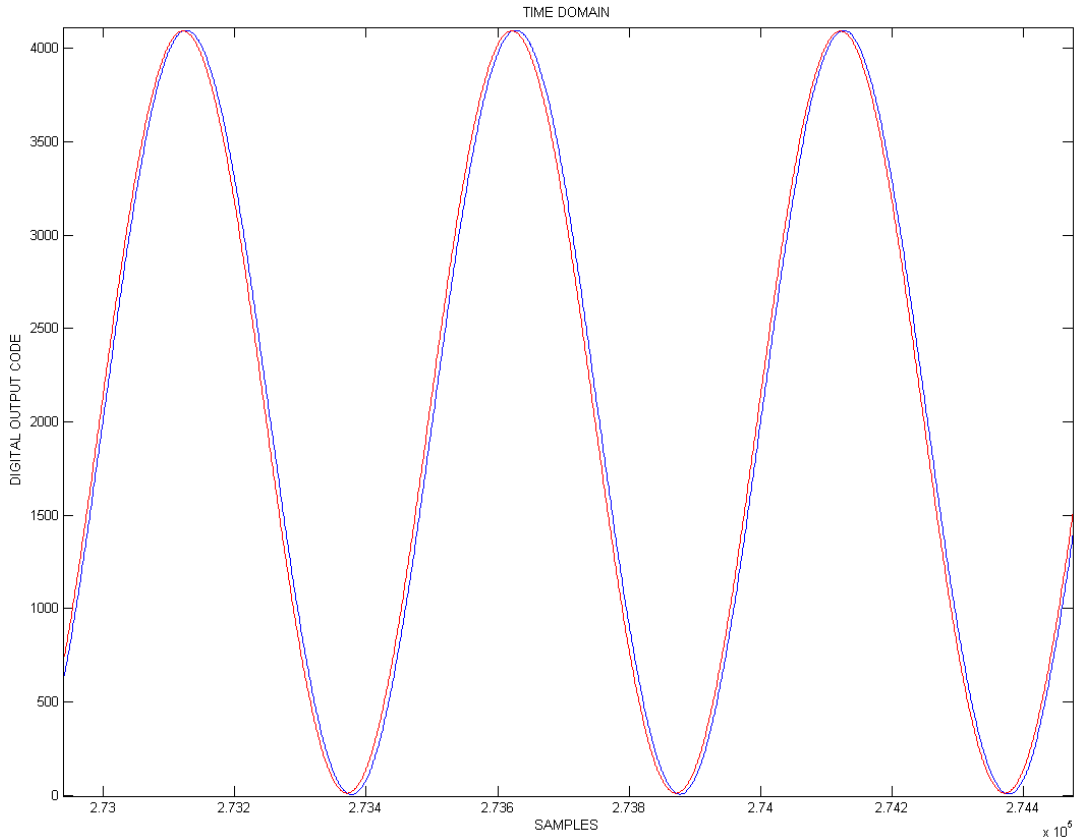
2/3/4. On opening the AZ-switches from back to front the autozero-capacitors store offset from preamplifiers

ADC Lab-Results: Time-Domain-Signal

Test signal for ADC-performance-check:

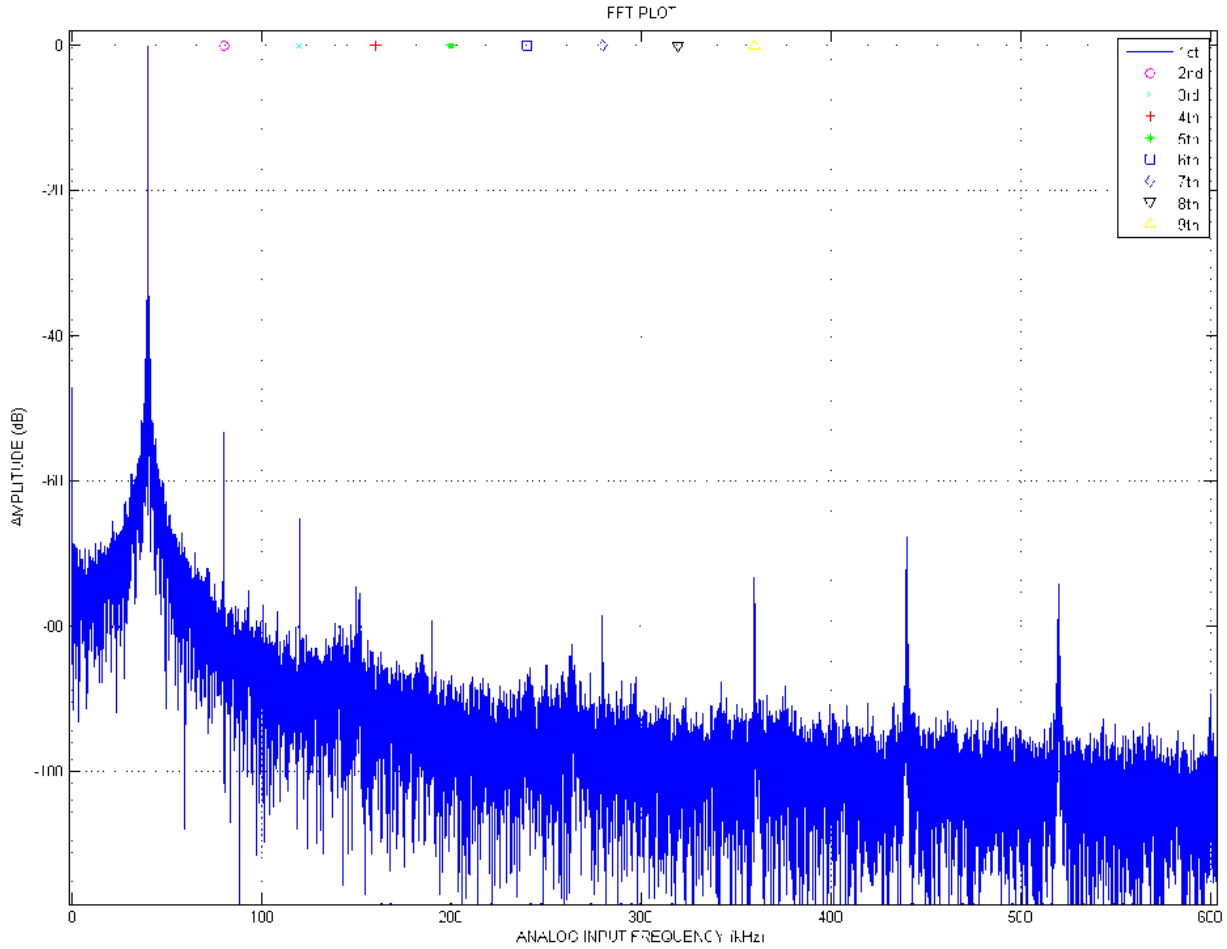
- clean sine (negligible distortion & noise)
- perfect full-scale amplitude
- long conversion period to acquire enough data

→ time domain signal (blue) with Sine Wave Fitting (red) from 512kSamples, f_S=20kS/s



ADC Lab-Results: FFT

Performance parameters can be calculated from the FFT of the conversion data:



FFT (512k Samples, 20kS/s)

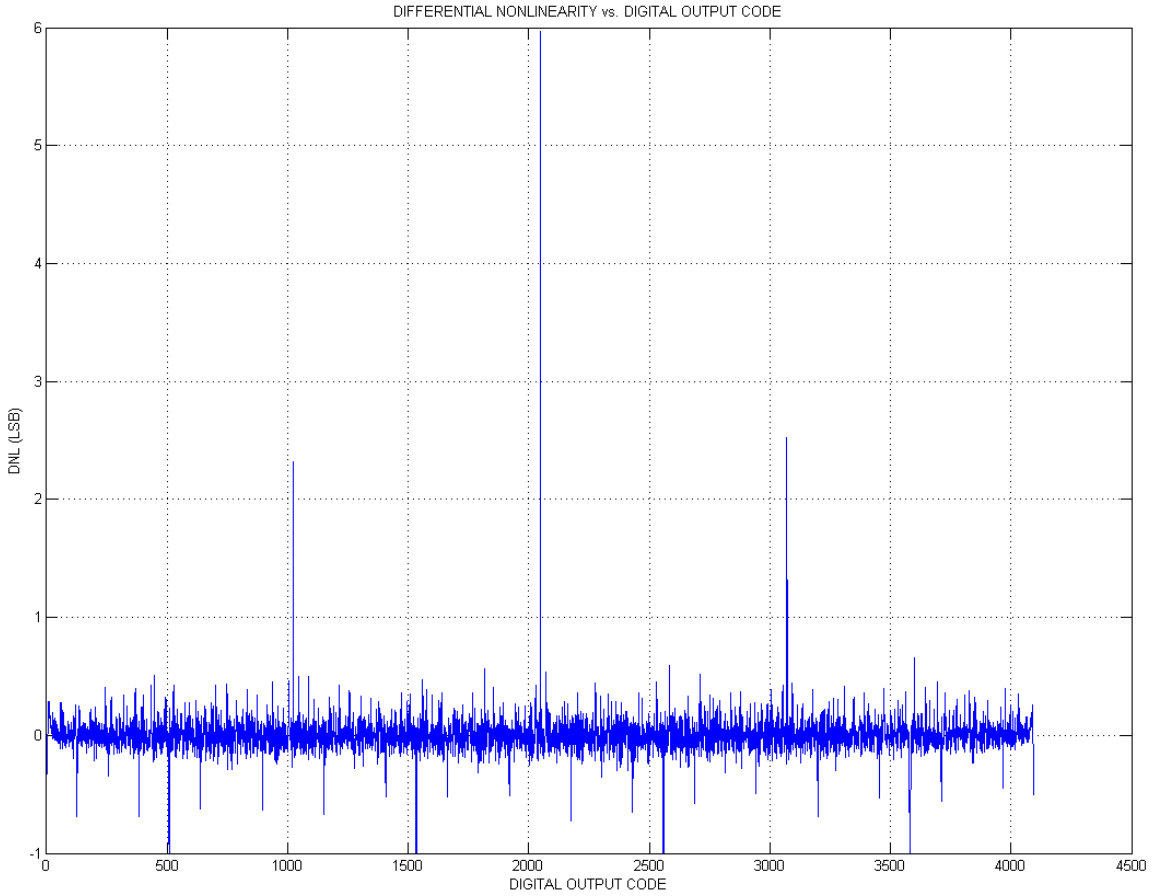
Calculated parameters:

Frq.:	39,9399Hz
A:	0,99976
SINAD:	51,2632 dB
ENOB:	9,1009
SNR:	51,2905 dB
THD:	-53,2483 dB
SFDR:	53,2557 dB @ 2

ADC Lab-Results: Differential Nonlinearity (DNL)

→ DNL: deviation in step sizes differing from ideal +1 LSB step

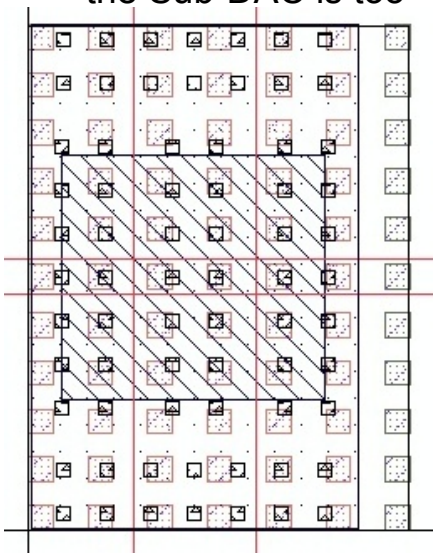
→ here: 6 LSBs → costs 3 bits of resolution → undesirable



DNL of the ADC (512k Samples)

Reason:

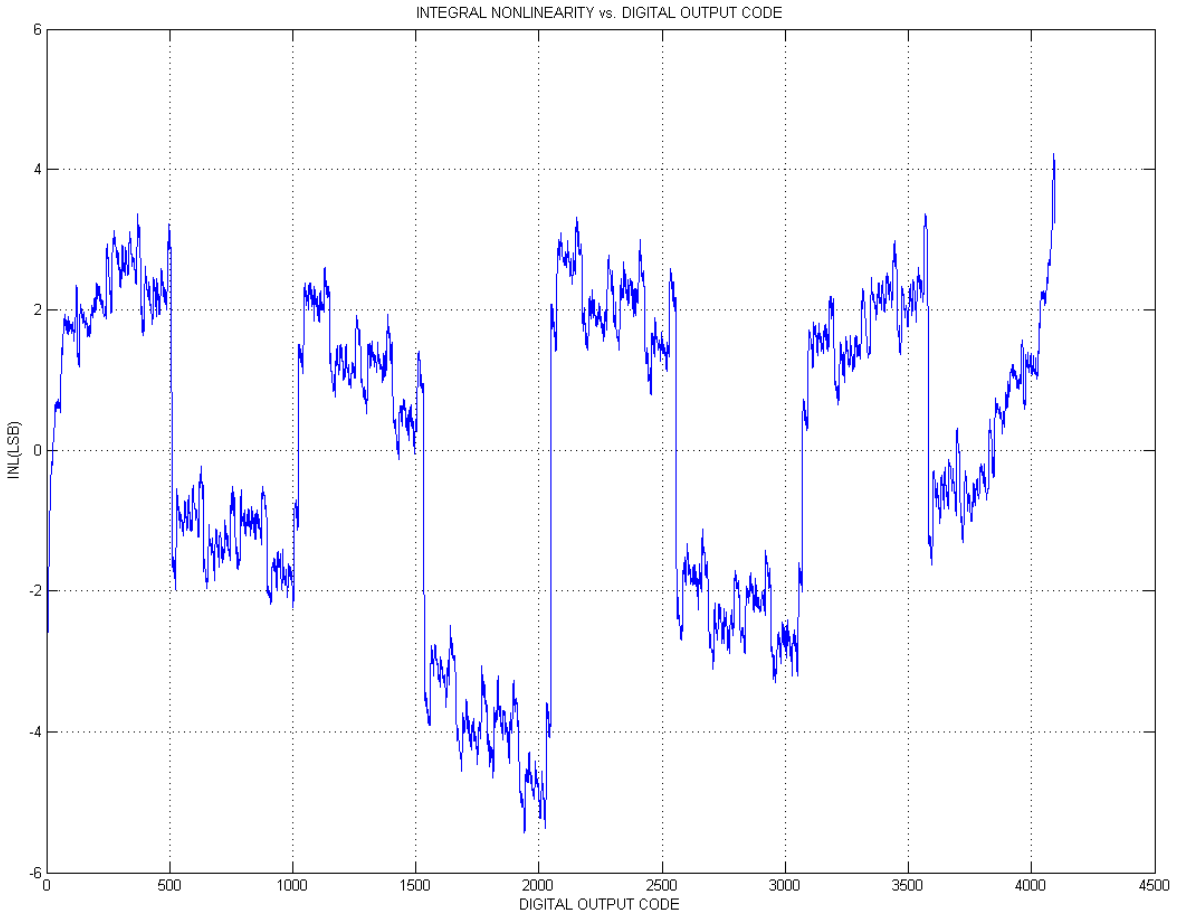
mandatory metal-fill-structures on chip increases capacitance of the single elements (C_{nom}=104fF) → the scaling capacitor of the Sub-DAC is too



single capacitor element with fill structure

ADC Lab-Results: Integral Nonlinearity (INL)

- → INL: deviation from the ideal step value
- → here: 6 LSBs in either direction → costs 4 bits of resolution → possibly worse than in reality due to measurement errors

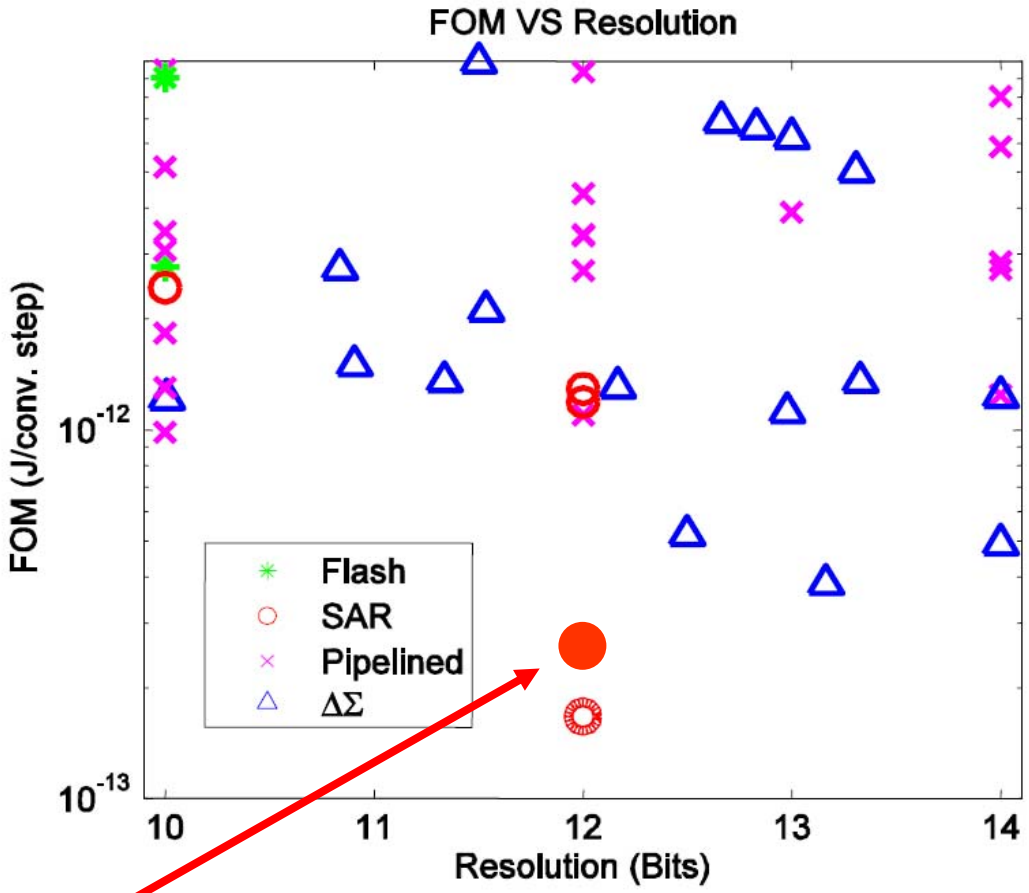


INL of the ADC (512k Samples)

ADC-Performance Comparison: Figure of Merit (FOM)

Relation of power, resolution and input frequency:

$$FOM = \frac{P}{2^{ENOB} 2F_{IN}}$$



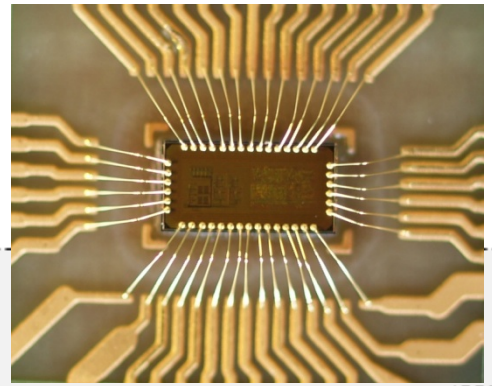
Source: IEEE, ISSCC 2006, session 12.5

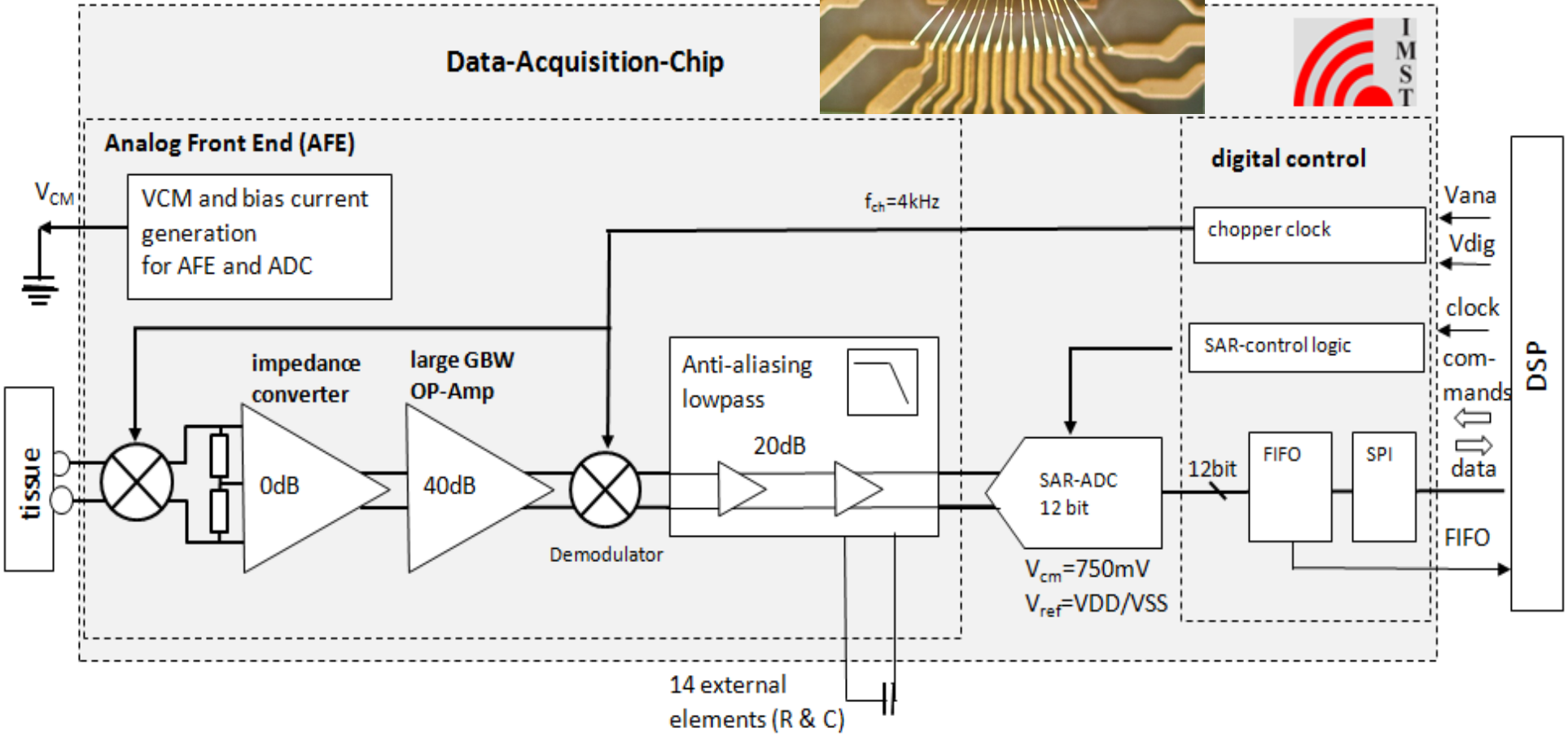
FOM for the Ultrasponder-ADC:

$$FOM = \frac{P_{ADC}}{2^{ENOB} 2f_{in}} = \frac{1.5V \cdot 19.2uA}{2^{11} \cdot 2 \cdot 27.5kHz} = 2.56 \cdot 10^{-13} \frac{J}{convstep}$$

Summary: Ultrasponder Data-Acquisition-Chip

- process technology 130nm





Performance summary

	Parameter	Symbol	Value	Notes
SYSTEM	supply voltage	AVDD, DVDD	1.5V	±5%
	temperature range	T	27° to 42°C	body temperature
	system clock frequency	f_{clk}	max. 1MHz	from crystal (100ppm)
	common mode DC level	V_{CM}	750mV	VCM- generation on chip
	total power consumption	P_{tot}	~400uW	
AFE	gain	A_{AFE}	60dB	using chopping technique
	input frequency range	$f_{IN,AFE}$	DC-70Hz	
	chopper frequency	f_{CH}	4kHz-6kHz	
	input voltage range	$V_{IN,PP}$	1uV-1mV	
	anti aliasing low pass corner frequency	$f_{c,AALP}$	70Hz	4th order active, 20dB gain, external passive elements
ADC	resolution	ENOB	8-9 bit	targeted 12 bit
	ADC input voltage range	$V_{IN,ADC}$	0.1 to +1.4V	positive differential input voltage
	input frequency range	$f_{IN,ADC}$	0.1Hz-27.5kHz	ADC in stand-alone mode
	max. sampling frequency	$f_{S,max}$	55.5kS/s	NOTE: $f_{in,max} \leq f_S/2$
	power consumption of ADC only	P_{ADC}	28uW	FOM: 2.56e-13 J/conv-step
digital	Number of steps for SAR-control	N_{SAR}	18	autozero, bit-cycling, data-ready
	FIFO size	N_{FIFO}	100 words	1 word = 12bit
	SPI-clock	f_{SPI}	16kHz-10MHz	slave-mode

Questions?

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