ISMICT 2011– Montreux, Switzerland
Workshop: Ultrasound dedicated to medical applications
in the frame of the FP7 ICT European project ULTRAsponder

Ultra-low power digital processing for medical applications

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System-on-Chip & Digital IC Design

Integrated & Wireless Systems Division

CSEM – Swiss Center for Electronics and Microtechnology

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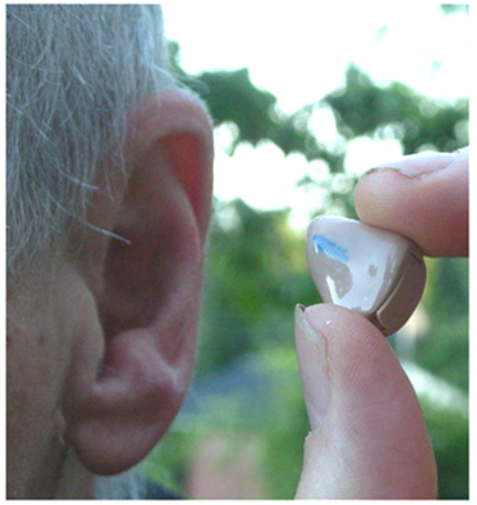
Quick introduction to CSEM

- private company, founded in the 1980's
- not for profit
- approx. 400 employees on 5 sites in Switzerland, HQ in Neuchatel
- 8 technical divisions:
  - microelectronics, photonics, nanotechnology, nanomedicine
  - robotics, system engineering, microsystems, thin film optics
- approx. 60 MCHF annual budget
- over 20 start-ups and spin-offs since 1995

Medical applications

- Ultrasound transponder implants
- Continuous ECG or multi-parameter monitoring
- Hearing aids
- Cochlear implants
- e-pills
- Other implants

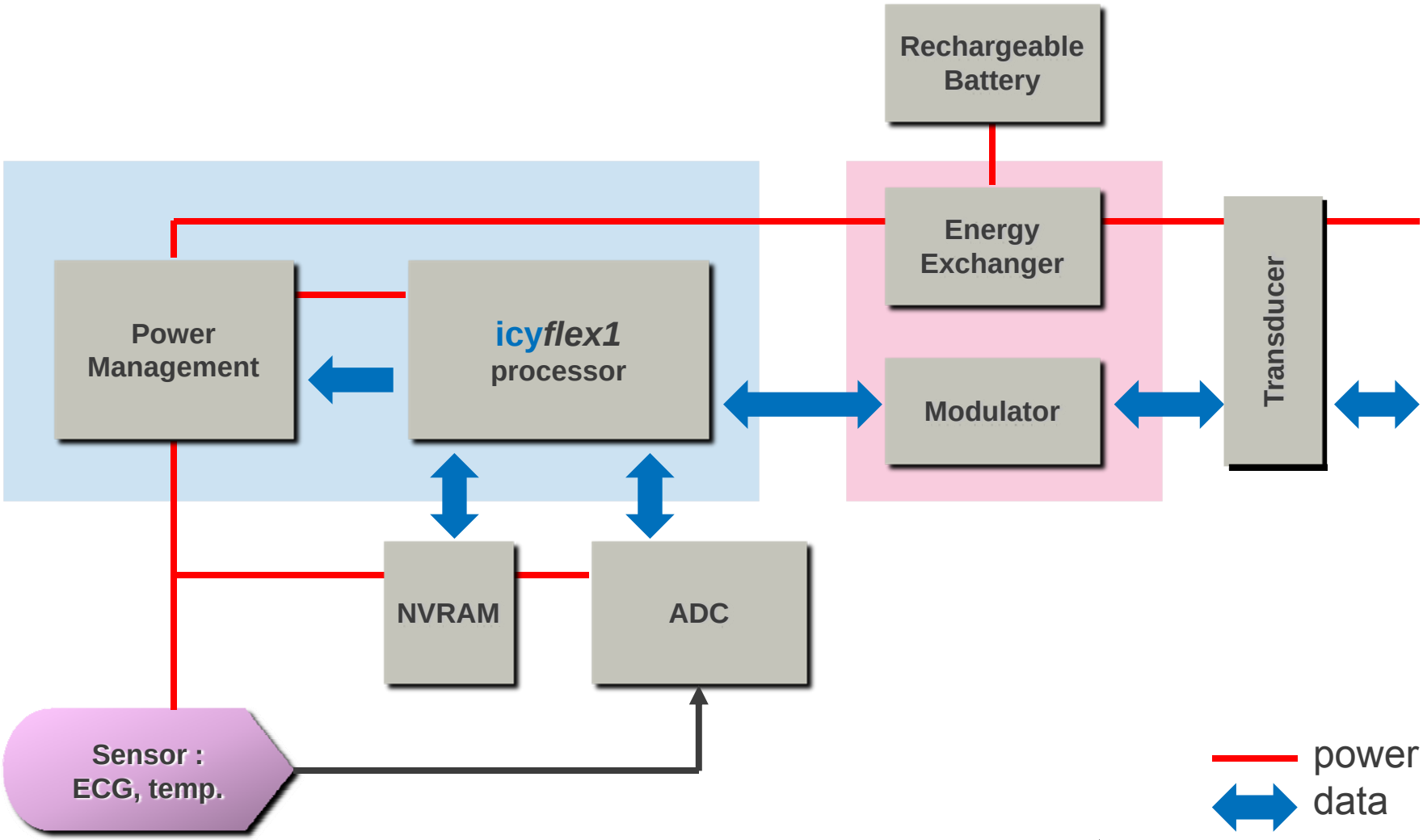


- Common SoC requirements:
  - extend battery life
  - local processing

System-on-Chip for wireless applications

- ULTRAsponder SoC for ultrasound operation:
  - ultra-low power processor + power management
- icycom for wireless sensor network:
  - RF transceiver 863-928 MHz with OOK, FSK, OQPSK modulation
    - TX: 40 mA, 10 dBm. RX: 3.5 mA, -100 dBm.
    - e.g. 200 kb/s, MSK, range of 5 km (free space)
  - 8-channel 10-bit ADC, 5 nC/sample
- new SoC for wireless Body Area Network:
    - TX: 2.0 to 3.5 mA, -30 to -3 dBm. RX: 3.5 mA, -100 dBm
    - e.g. 200 kb/s, MSK, range of 0.1 to 2 km (free space)

The ULTRAsponder system view



The ULTRAsponder core SoC – digital functions

- Processor:
  - **icy*flex1*** ultra-low power DSP/control processor
  - 120 µA/MHz at 1.0 V regulated power supply
  - runs at up to 3.2 MHz at 1.0 V in this SoC
  - SRAM: 96 kiBytes
- Other digital blocks:
  - DMA controller, JTAG tap, IRQ controller, bus controller
  - RTC, Timers, Watchdog, I2C, SPI, UART, GPIO
- Design For Test:
  - 4 scan chains, Memory Built In Self Test

The ULTRAsponder core SoC – power management

- Power supply:
  - 1.0 V – 3.6 V
- Power management to supply power to the SoC and external devices
  - programmable voltage regulator (64 steps, 0 – VBAT)
  - voltage divider by 2
  - digital voltage regulator 1.0 V
  - 2 voltage multipliers (2.7 V): max 10 µA and 13 mA currents
  - separate power supply per bank of pads

The ULTRAsponder core SoC – power modes

Mode	Processor	Digital blocks	RAM blocks	Clock	Power
normal	running	all clocked	all on	3.2 MHz	120 µW/MHz + RAM
sleep	clock gated	some clocked	some on	3.2 MHz	2-4 µW
hibernation	power off	only RTC on	all off	32 kiHz	1 µW

Ultra low-power processors at CSEM

- CSEM has a long history of designing low-power processors
  - Watch processors: PUNCH (1993), µPUS, Combo (1982), ...
  - CoolRISC, licensed to Semtech, Swatch group, TI, ...

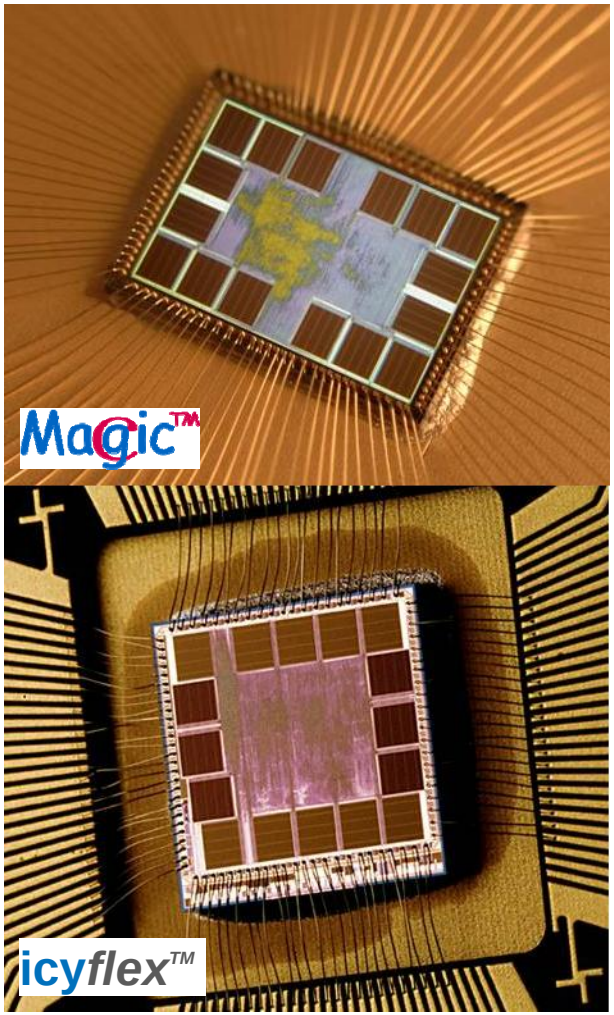
- Powerful new processors with ultra low power consumption
  - 2005: Macgic, a 16/24-bit DSP (4 MAC)
  - 2006: **icy*flex1***, a flexible processor for DSP/control applications
  - 2009: **icy*flex2***, a smaller processor for control applications
  - 2009: **icy*flex4***, a scalable processor for DSP/control applications

Macgic and **icy*flex*** are registered trademarks of CSEM

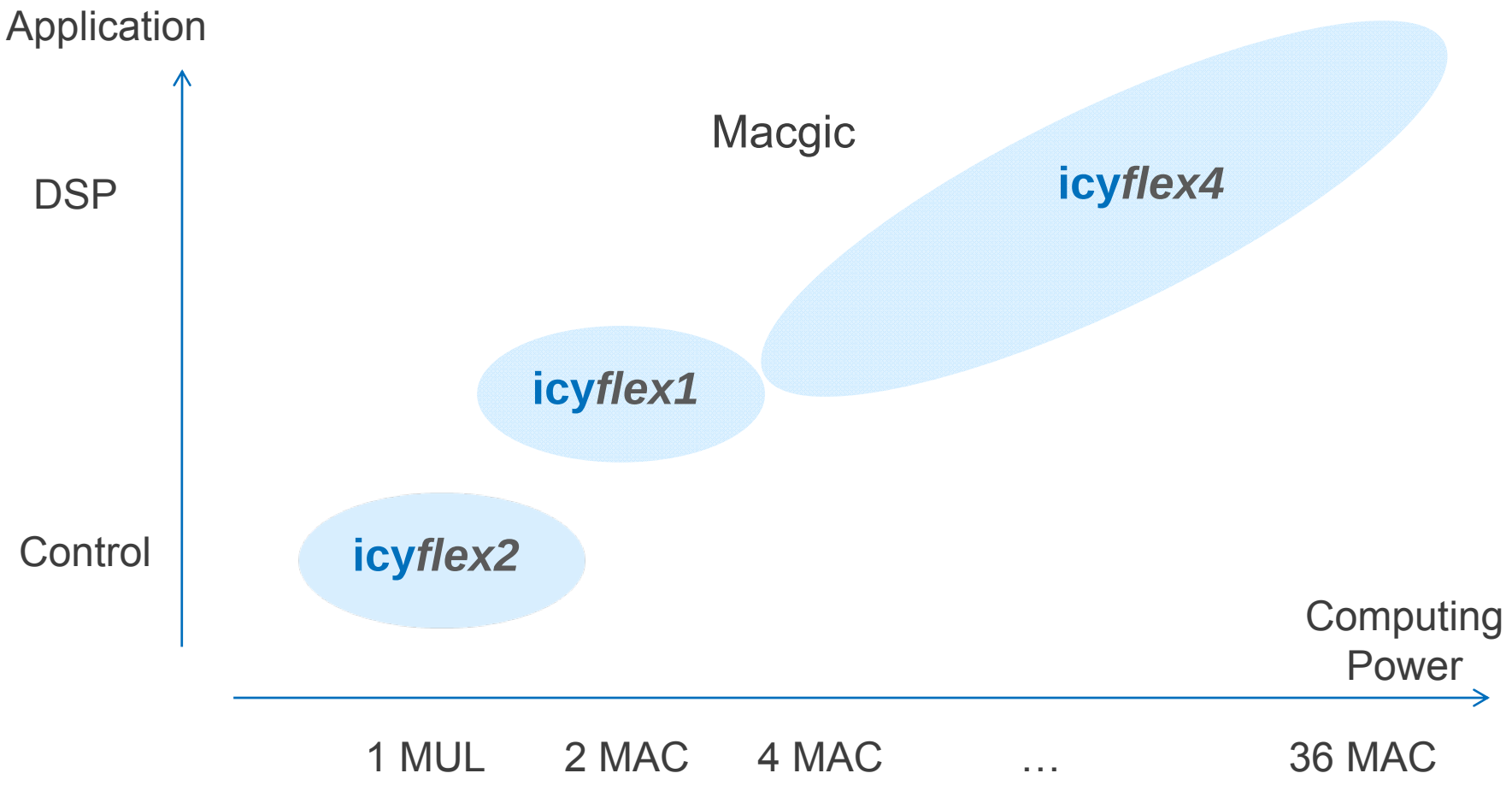
Ultra-low power processors

Macgic and the icyflex processors are optimized for power consumption:

- customizable (in VHDL)
- configurable (at run-time)
- architecture
- instruction set
- latch-based design
- clock-gating



Processor selection

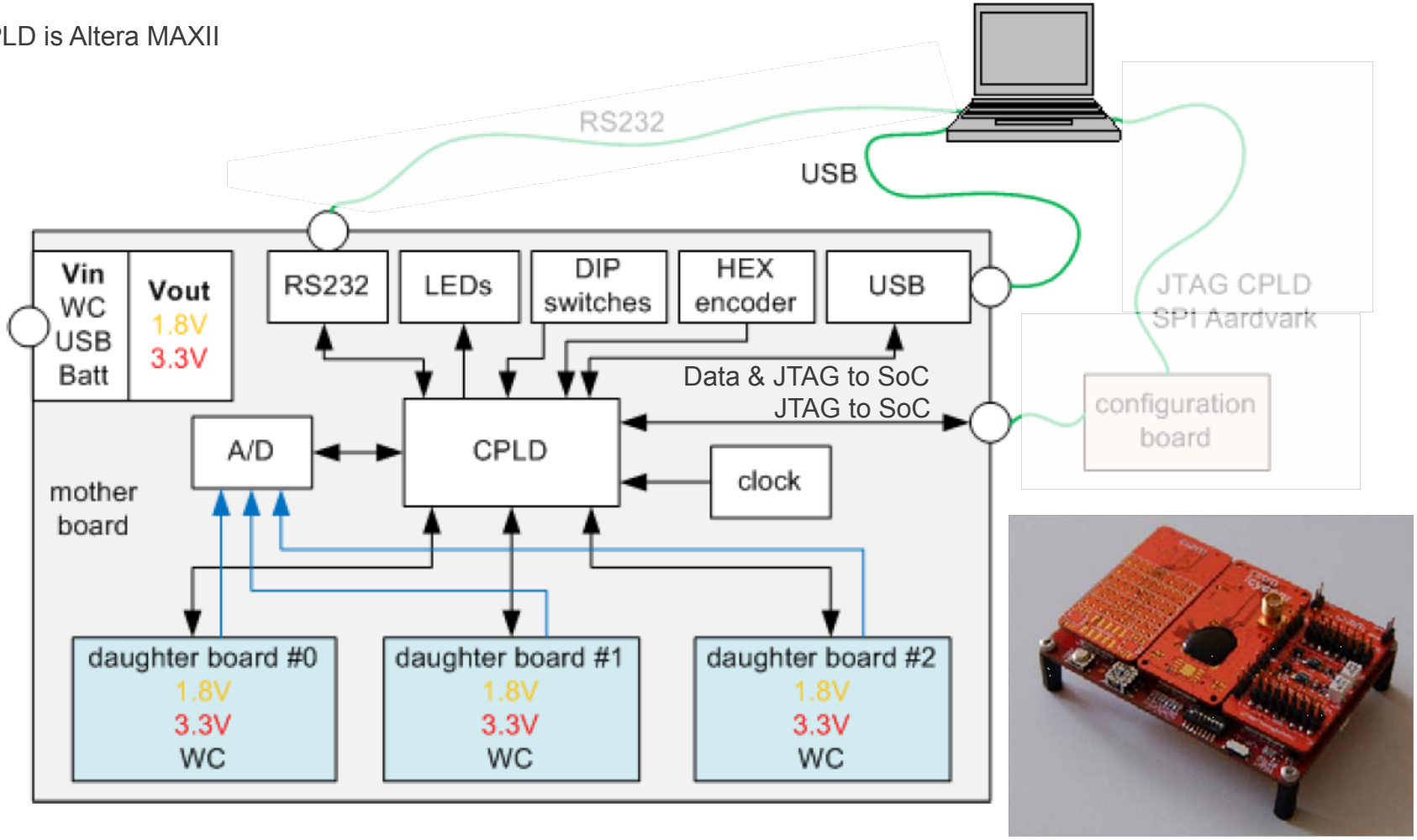


icy*flex* software development kit

- GNU C compiler (gcc) v 4.2.4
  - **icy*flex*** instruction parallelism supported by latest releases of gcc
  - libc and libm from RedHat's NewLib
  - software implementation of IEEE floating-point standard
- GNU assembler / linker (binutils), v 2.20
  - BFD / ELF32 object file format
  - Binary, SREC, IHEX memory image file formats
- GNU debugger (gdb), v 6.7.1
  - Mode 1: instruction set simulator of the **icy*flex*** core
  - Mode 2: On-Chip Debug (OCD) through a JTAG interface
- **icy*flex*** instruction set simulator (ISS), written in C++
  - Phase-accurate, pipelined
  - Wrappers to SystemC, VHDL (Modelsim), Matlab/Simulink
- Eclipse integrated development environment, v Helios
  - CDT C/C++ IDE plug-in
  - **icy*flex*** plug-in

icyflex hardware development kit

CPLD is Altera MAXII



Overview of the icy*flex1* processor

Characteristics of the icyflex1 architecture

- Simplicity
  - 3-stage pipeline
- Efficiency ➔ parallelism
  - Data-level
  - Instruction-level

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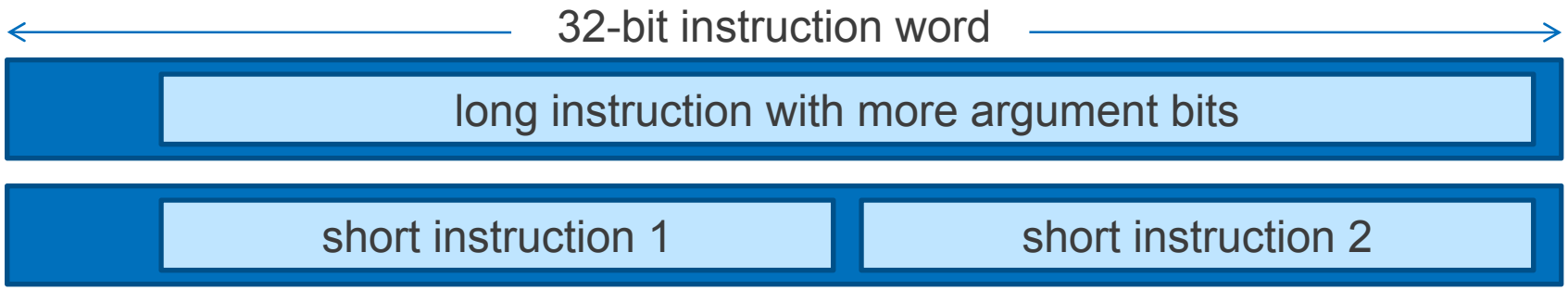

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  - Data-level:
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  - Instruction-level:
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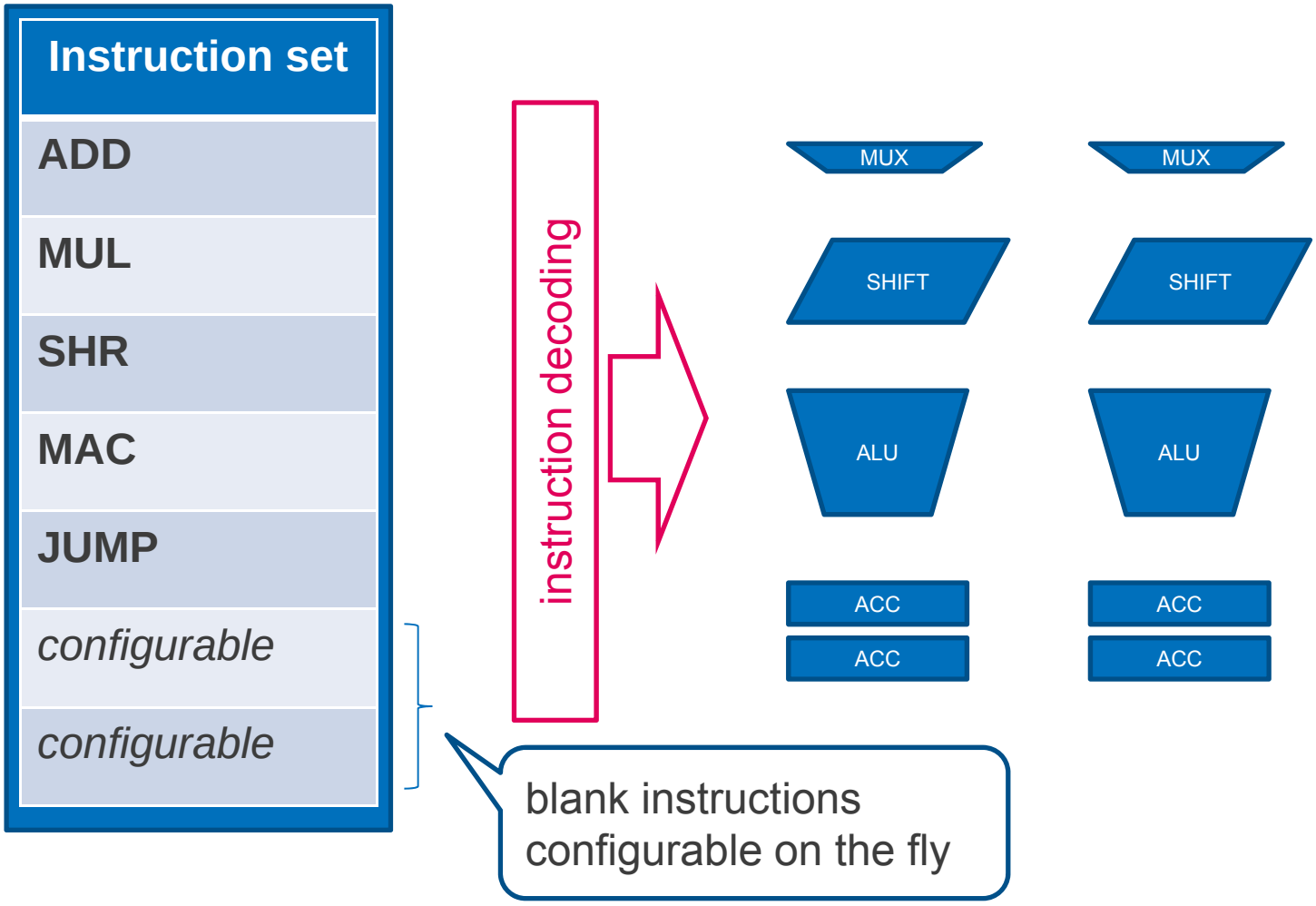
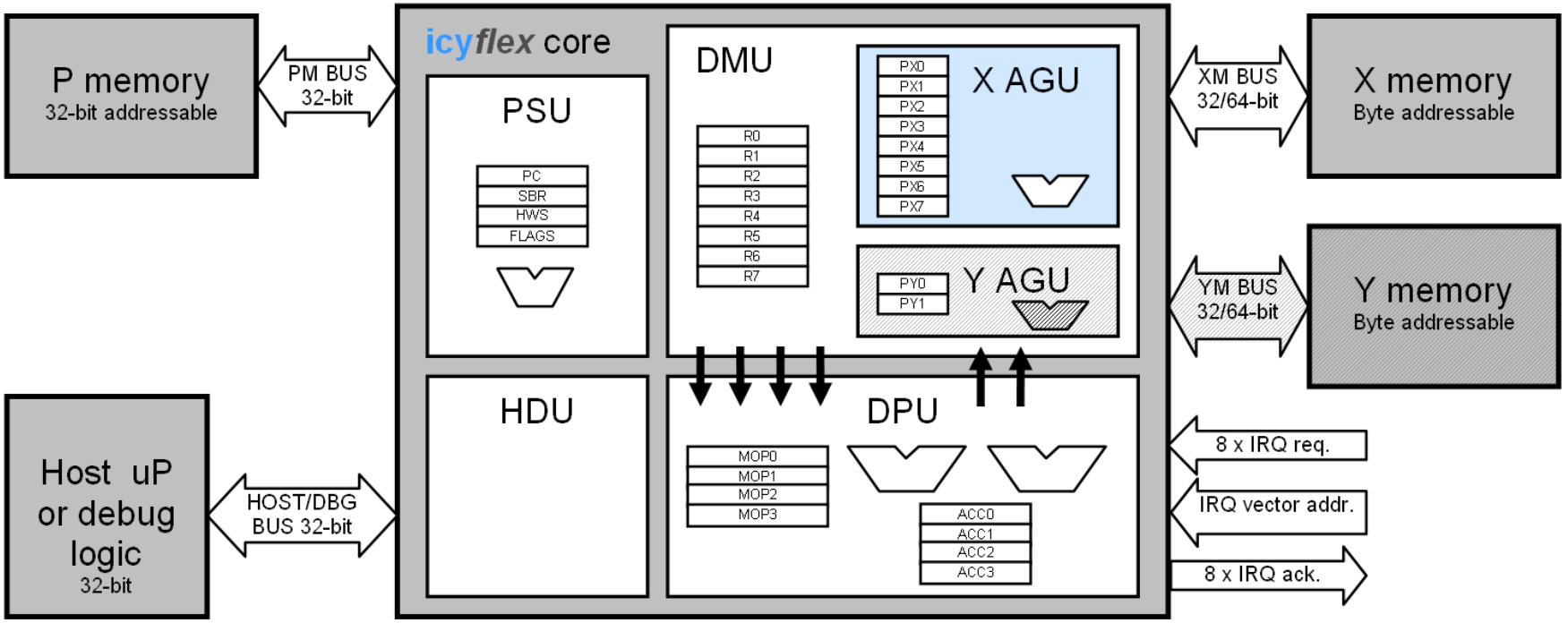
    - New instructions can be configured at run-time

Reconfigurable instructions and addressing modes

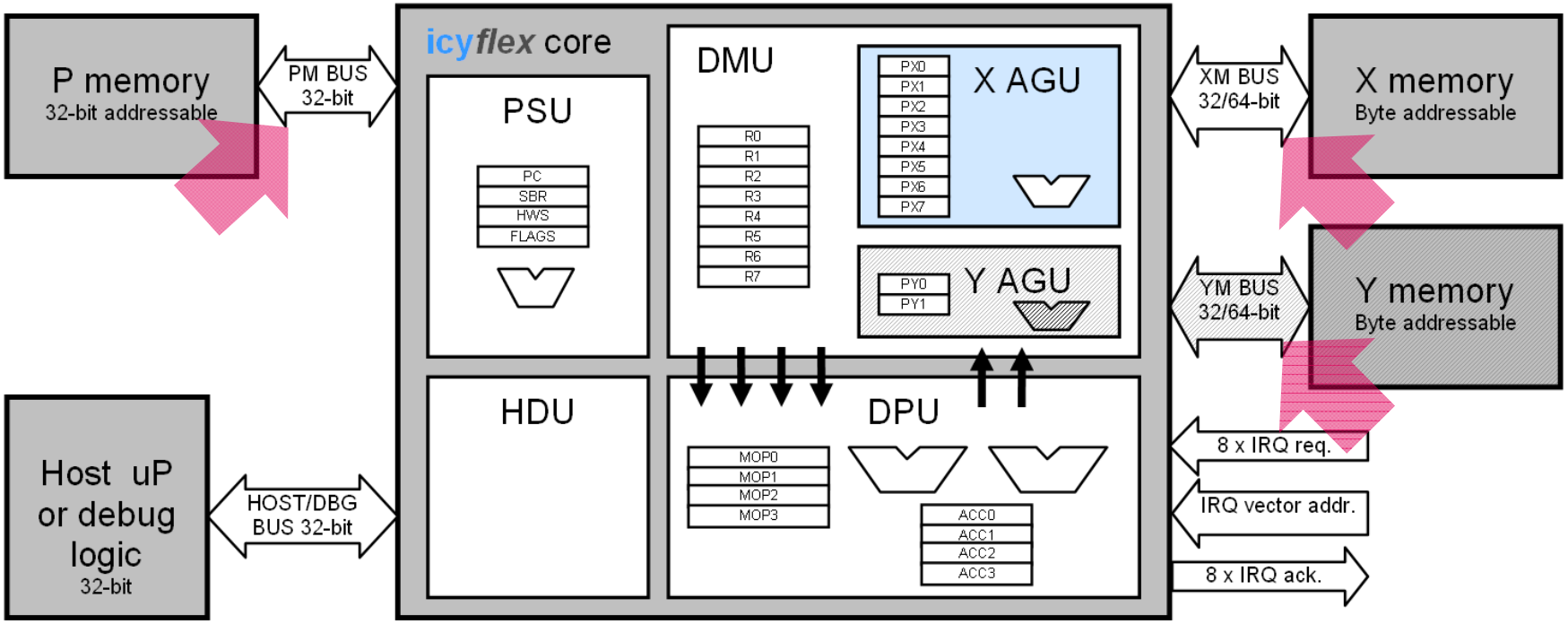


icyflex1 architecture



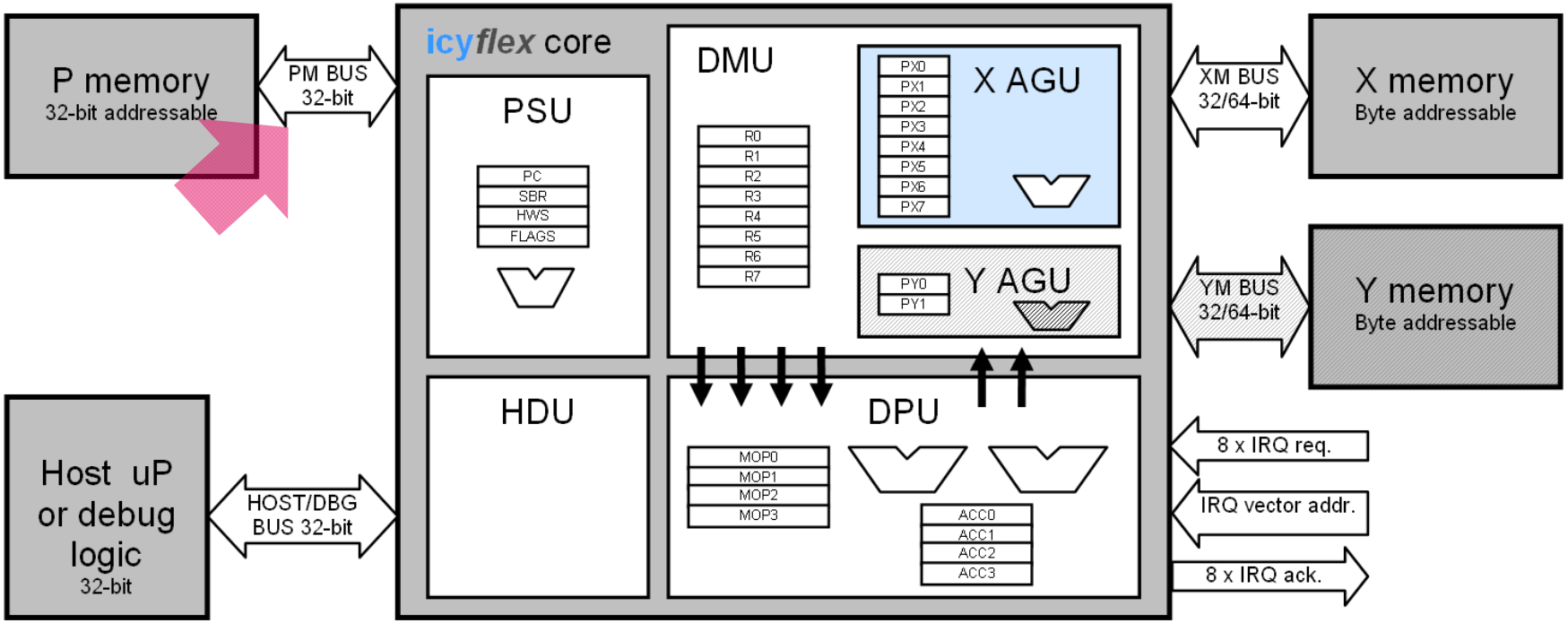
icyflex1 architecture

3 separate busses ➔ up to 3 parallel accesses every clock cycle
less clock cycles ➔ less power consumption



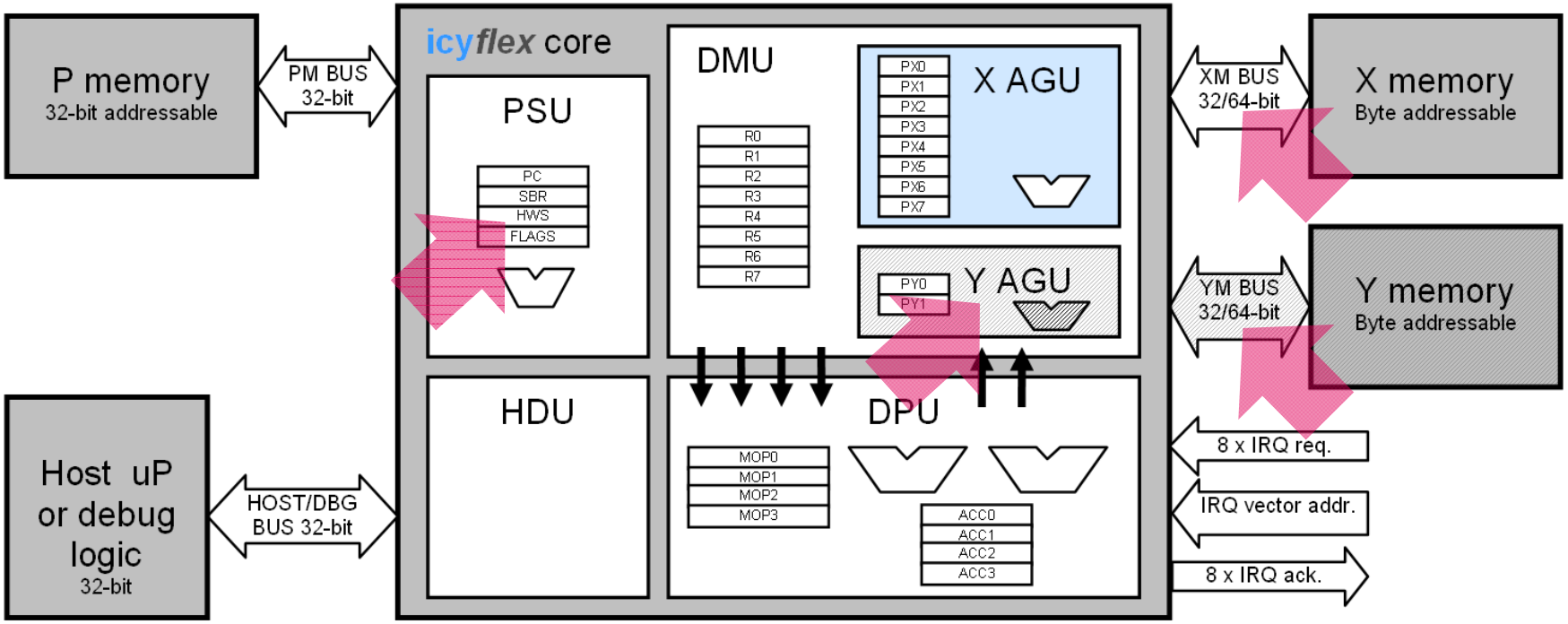
icyflex1 architecture

32-bit instruction word ➔ optimized instruction set avoids VLIW
shorter instruction word ➔ less power consumption



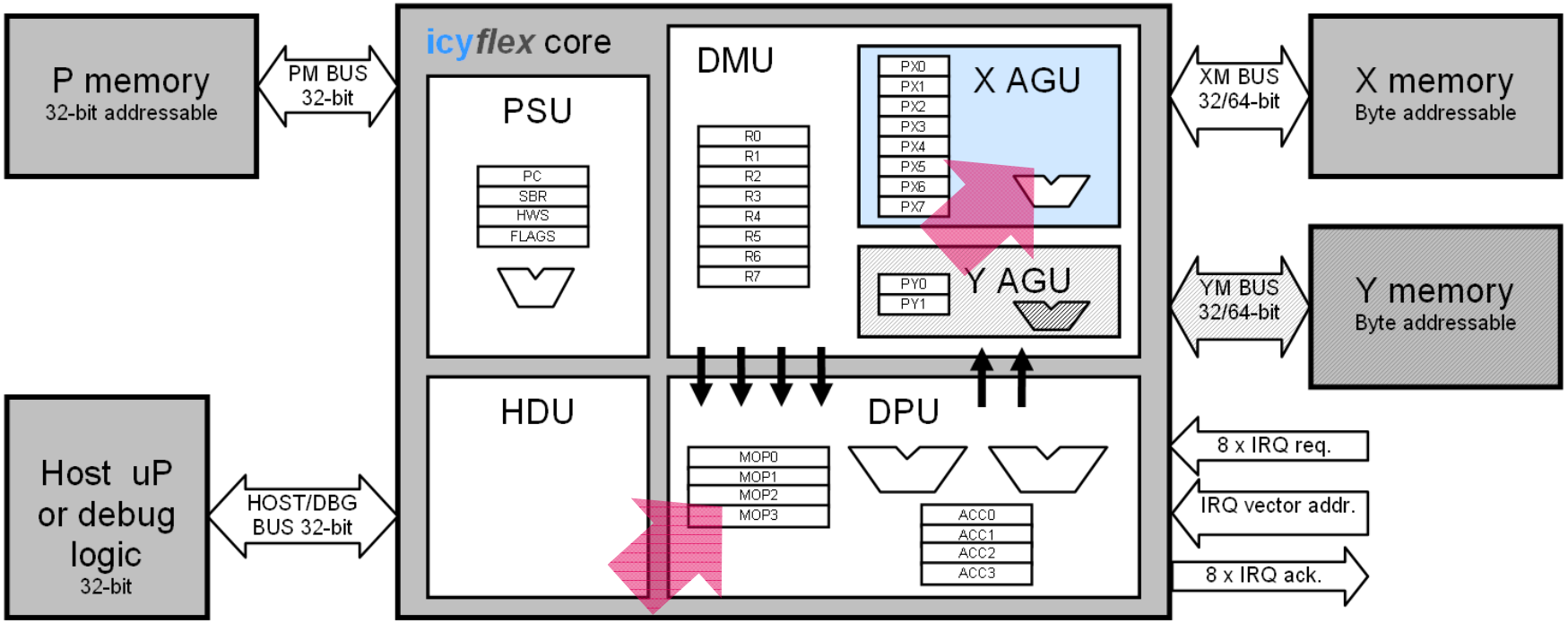
icyflex1 architecture

customizable at synthesis ➔ busses can be shrunk, blocks can be removed
only useful logic is integrated ➔ less power consumption



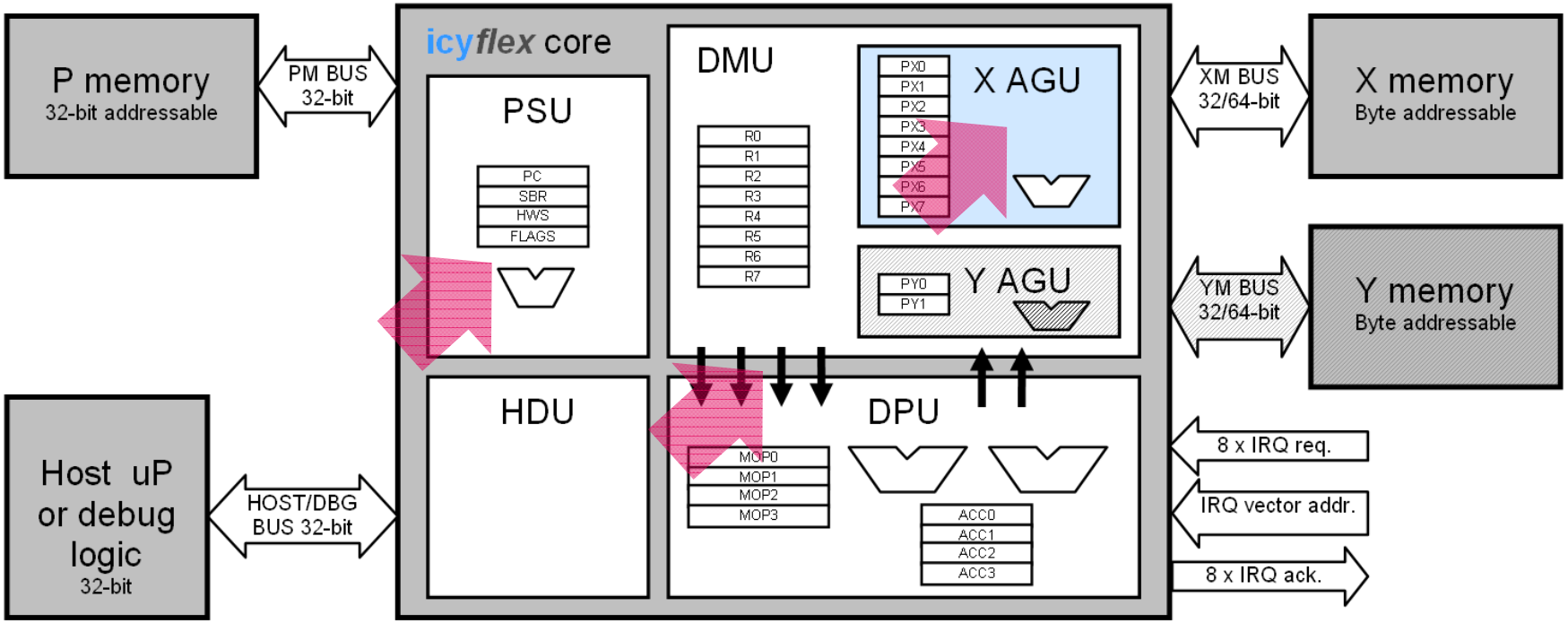
icyflex1 architecture

reconfigurable instructions and addressing modes ➔ execute less instructions ➔ less clock cycles, smaller program memory, less power consumption



icyflex1 architecture

DSP-type features: zero-overhead hardware loop, complex addressing modes, high and balanced throughput



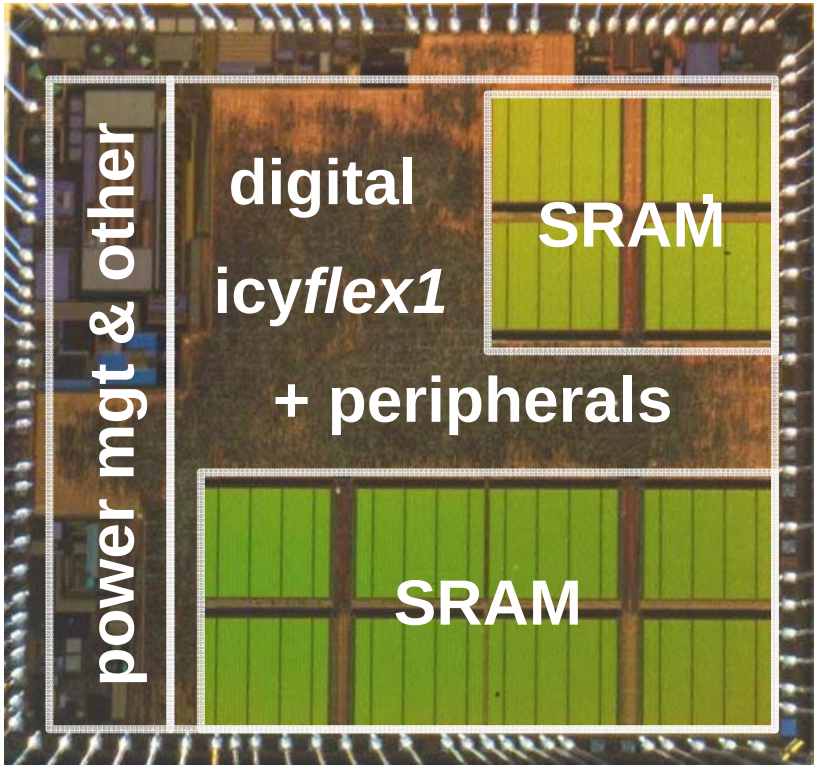
Performance summary

		icy*flex1*	icy*flex2*	icy*flex4*
MAC (or MUL) units		2	(1)	4 + 4 VPS
Data size [bits]		16/32	16/32	16/32
Pipeline depth		3	5	5-8
Software tools		gcc / gas	gcc/gas	gcc / gas
k Gates		110	40	130 + 90 VPS
Max. ops/cycle		16	6	33 + 31 VPS
Max. freq. [MHz]	180 nm	50		
	LP RVT 90 nm		180	180
Avg. Power [µW/MHz]	180 nm	**120**	30	
	65 nm		6	10 to 150*

*) VPS=2, FFT radix-4 64 points

The Ultrasponder core SoC

- Integrated in TSMC 180 nm generic CMOS process
- 5 x 5 mm^2
- 12 blocks of 8 kiB ultra-low power SRAM
- mix of thin and thick gate transistors



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Thank you for your attention!

Questions?

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